TECHNICAL MANUAL

SEQUENTIAL CIRCUITS INC

MODEL 100
Manual No. TM100A

PRO-ONE SYNTHESIZER

TECHNICAL MANUAL

by Stanley Jungleib

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Manual No. TM100A
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SECTION 1

FUNCTIONAL TESTS

1-0 INTRODUCTION

This section contains procedures for complete functional testing of the Pro-One. The functional tests check all signal paths and the range of the oscillators. A flow-chart for selectively checking tuning is on page 1-12. To correct oscillator tuning, see the Service procedures in Section 5.

Instruments to be serviced should be completely tested beforehand. This will reveal related or unrelated malfunctions, and provide a basis for troubleshooting. If a trim can't be achieved service will certainly be required. In such cases, consult the theory of operation and diagrams in Section 2, and schematics in Section 3 to isolate the failure.

Mechanical procedures are in Section 4. When operating disassembled it can be difficult to read the controls: Figure 3-1 may be of help. Also, when disassembled it is often convenient to leave the wheel cable disconnected. The Pro-One will operate normally, that is, without pitch bend or modulation.

These procedures are presented in the order recommended for a Pro-One assumed to be completely operational. Real-world problems may require you change the order of some tests. Therefore each is written to be performed independently.

You must play the Pro-One throughout these tests (or use the ascending and descending scales preprogrammed into SEQ 1 and SEQ 2 on power-up). All tests are performed by ear, the object generally being that the knobs adjust smoothly and switches work. Toggle the panel switches repeatedly to check for intermittents.

1-1 PREPARATION

1. Connect headphones, or mono cable between back panel AUDIO OUT jack and power amplifier.

2. Check back panel 115/230 line voltage selector.

3. Check that back panel power switch is off.

4. If operating disassembled, testing may be facilitated by placing the knobs lightly back on their shafts.

5. Connect power cable to properly-grounded outlet.

6. Switch power on.

WARNING! LETHAL VOLTAGE IS PRESENT IN THE POWER SUPPLY AREA ON THE PCB (IN EARLIER MODELS) OR ON THE BACK PANEL (IN LATER MODELS).

7. Center MASTER TUNE and PITCH wheel and set MOD wheel to minimum (unless the wheel cable is disconnected).

8. Adjust VOLUME as required, below.

1-2 KEYBOARD TEST

1. Patch according to Figures 1-1 or 1-2. The essential features of these patches are a fully "open" AMPLIFIER and FILTER, the sawtooth of one oscillator is on, and there is no modulation.

2. Check that all keys work. Make a note of scratchy, intermittent, or inoperative keys. Oxidation, particularly of lesser-used keys, can cause keys to go "dead," and may be aggravated by ambient conditions or handling. Check also for contact bounce by hitting each key hard and repeatedly while listening for break-up or double triggering.

For either condition, cleaning or careful readjustment of the "J-wires" is often all that is necessary. After the top panel is removed, the keyboard can be detached from the bottom panel for cleaning by simply removing four screws. Wipe the contacts carefully with an alcohol- or freon-wetted cotton swab. Don't use any abrasive techniques, as this will simply remove the gold plating. Replacement J-wires can be ordered as SCI #S-051.

3. If the keyboard doesn't work at all, check its connector. The GATE LED should light whenever a key is pressed. If still there is no sound, check Final VCA (para. 1-8).

4. Switch DRONE on. You should hear a continuous tone. The frequency will change as you play various keys, but the tone itself is not interrupted. Switch DRONE off.

5. Switch REPEAT/EXT on. The frequency of the last key played repeats at a rate set by the LFO/CLOCK FREQUENCY knob. Keys will not be heard when played, but repeated pitch will change. Switch REPEAT/EXT back to NORMAL.

6. To check or demonstrate low-note priority, hold a key and hit one above it. The higher key will not sound. Now hold the higher key and hit the lower one. The lower key sounds when pressed.

5. Switch MODE from NORMAL to RETRIG. Note that this switches from low-note to last-note priority. The newest key sounds though a lower key may be held.

6. Hold several notes and switch ARPEGGIATE UP, then UP/DOWN to check function. While arpeggiating, switch up SEQUENCER RECORD and remove hand from keyboard. The arpeggiator should remain "latched." Switch ARPEGGIATE off.

7. With SEQUENCER RECORD still on, select SEQ 1 and record a sequence. Play it back. Repeat for SEQ 2.

1-3 OSCILLATOR A TEST

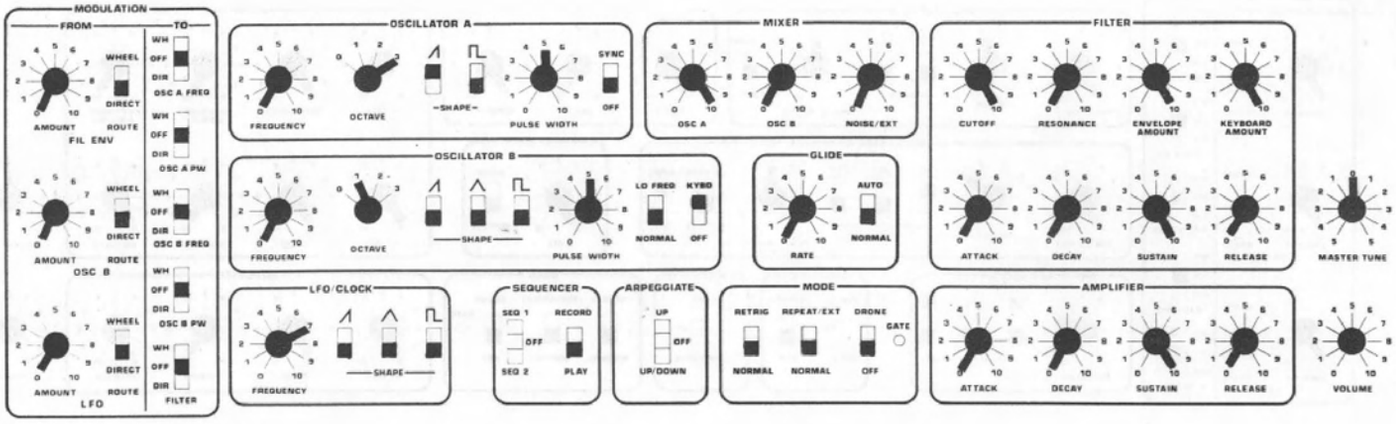


Figure 1-1
OSC A TEST PATCH

1. Patch according to Figure 1-1.

2. Check that OSC A FREQUENCY knob range exceeds one octave. For reference, play C2 (which is one octave below the highest key, C3) and remember pitch. Then hold C1 and raise OSC A FREQ. The pitch should increase smoothly, approaching the reference pitch at 7 - 8 on the dial. At 10 the pitch should be at least a whole step above the reference.

3. Turn OSC A FREQ to 0. Check OSC A OCTAVE switch function by playing C2 and switching octaves down to 2, 1, and 0. NOTE: When switching octaves with a key depressed, it is normal to hear the pitch "jump" between octaves.

4. Switch OSC A OCTAVE to 2, and switch OSC A SYNC on. Rotate OSC A FREQ knob 0 - 10 to check sync function.

5. Switch OSC A SYNC off. Switch OSC A SAWTOOTH off. Switch OSC A PULSE on. The difference between the "brassy" sawtooth and "woody" pulse should be obvious. Rotate OSC A PULSE WIDTH knob 0 - 10, listening for the timbral effect of varying harmonics. The pulse will degenerate to dc (or very nearly dc--99% duty cycle) at the extreme knob settings, resulting in no (or very little) sound. Find the setting where the second harmonic drops out (50% duty cycle). This normally occurs between dial markings 5 and 6.

1-4 OSCILLATOR B TEST

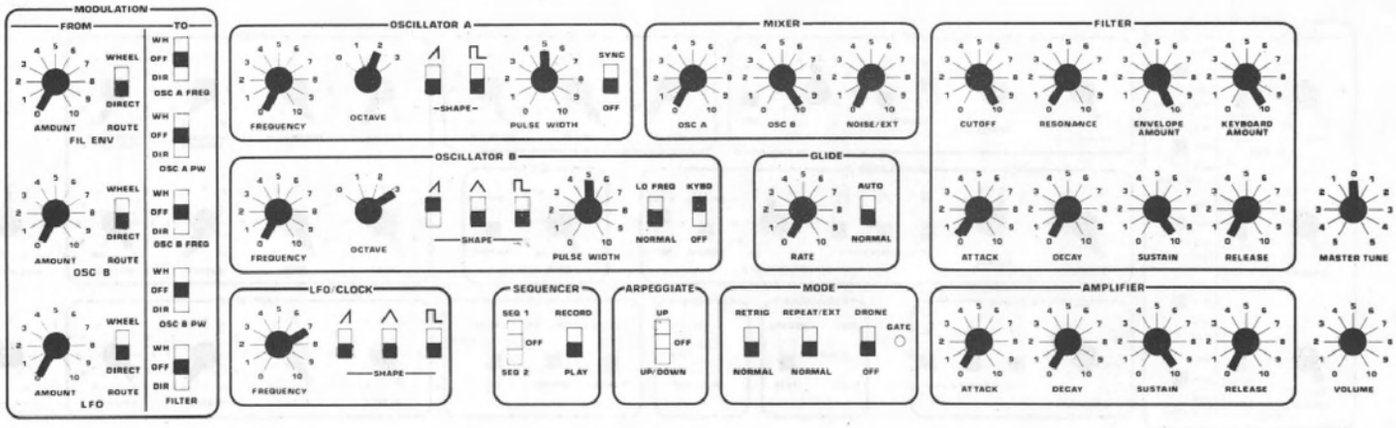


Figure 1-2
OSC B TEST PATCH

1. Patch according to Figure 1-2.

2. Check that OSC B FREQUENCY knob range exceeds one octave. For reference, play C2 and remember pitch. Then hold C1 and raise OSC B FREQ. The pitch should increase smoothly, approaching the reference tone at 7 - 8 on the dial. At 10 the pitch should be at least a whole step above the reference.

3. Turn OSC B FREQ to 0. Check OSC B OCTAVE switch by playing C2 and switching octaves down to 2, 1, and 0. NOTE: When switching octaves with a key depressed, it is normal to hear the pitch "jump" between octaves.

4. Switch OSC B OCTAVE to 2. Switch OSC B SAWTOOTH off. Switch OSC B TRIANGLE on. The difference between the "brassy" sawtooth and "dull" triangle wave should be obvious. The triangle waveshape has very little harmonic energy. Switch OSC B TRIANGLE off.

5. Switch OSC B PULSE on. Rotate OSC B PULSE WIDTH knob 0 - 10, listening for the timbral effect of varying harmonics. The pulse will degenerate to dc (or very nearly dc--99% duty cycle) at the extreme knob settings, resulting in no (or very little) sound. Find the setting where the second harmonic drops out (50% duty cycle). This normally occurs between dial markings 5 and 6.

6. Switch OSC B LO FREQ on. Raise OSC B FREQ to about 6 to more easily hear OSC B "track" the keyboard at low frequencies. NOTE: The OSC B LO FREQ switch extends OSC B's FREQ range to sub-audio. It is therefore normal that if OSC B FREQUENCY is set to 10, the LO FREQ switch will appear to have no effect. Switch OSC B LO FREQ to NORMAL.

7. Switch OSC B KYBD off and check that OSC B ceases "tracking" the keyboard.

1-5 MIXER and NOISE TEST

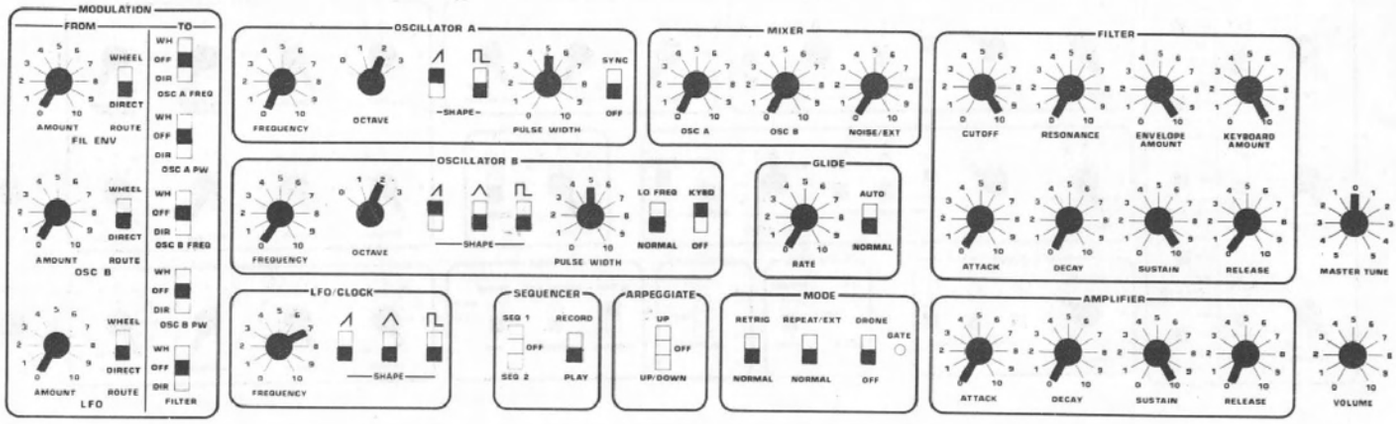


Figure 1-3
MIXER and NOISE TEST PATCH

1. Patch according to Figure 1-3.

2. Hold a key and turn MIXER OSC A knob 0 - 10. Check for smooth volume increase. Leave knob set to 0.

3. Turn MIXER OSC B knob 0 - 10. Check for smooth volume increase. OSC B should be as loud as OSC A. Leave knob set to 0.

4. Turn MIXER NOISE/EXT knob 0 - 10. Check for smooth noise volume increase. (Since noise is unpitched, it does not track the keyboard). Leave knob set to 0.

5. External audio input is checked during the BACK PANEL test (para. 1-10).

1-6 PITCH WHEEL AND GLIDE TEST

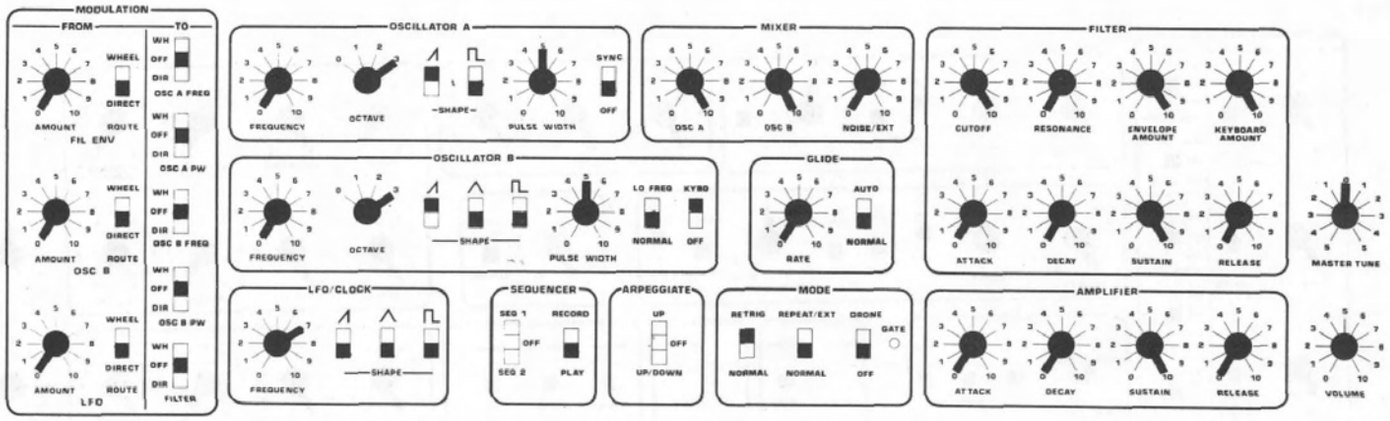


Figure 1-4
PITCH WHEEL and GLIDE TEST PATCH

1. If the wheel cable has been disconnected, switch power off and reconnect to test PITCH wheel. Otherwise, skip steps 3 and 4.

2. Patch according to Figure 1-4.

3. At this point you will probably hear "beats" resulting from the slight difference between OSC A and OSC B pitch. To "zero-beat," raise OSC A FREQUENCY (if OSC B is sharp) or OSC B FREQUENCY (if OSC A is sharp). It is not possible to maintain absolute zero-beat over more than a few seconds--but get as close as you can.

4. Slowly raise the PITCH wheel while listening for beats, then lower the wheel. Beating should not increase significantly as the pitch is raised or lowered. Increased beating probably indicates a difference in oscillator scaling, which can be corrected by retuning. The wheel range should be at least a fourth above and below the center pitch.

5. Check that the PITCH wheel is centered. Alternately play C3 and C0. There should be no detectable GLIDE. Now advance GLIDE RATE to 5 and repeat. This should yield a medium glide. Turn GLIDE RATE to 10 and repeat. It should take a minimum of 3 seconds to slew 3 octaves.

6. Switch AUTO-GLIDE on. Alternately play C3 and C0. There should be no GLIDE. Now hold C3 and play C0. This should activate GLIDE.

1-7 FILTER TEST

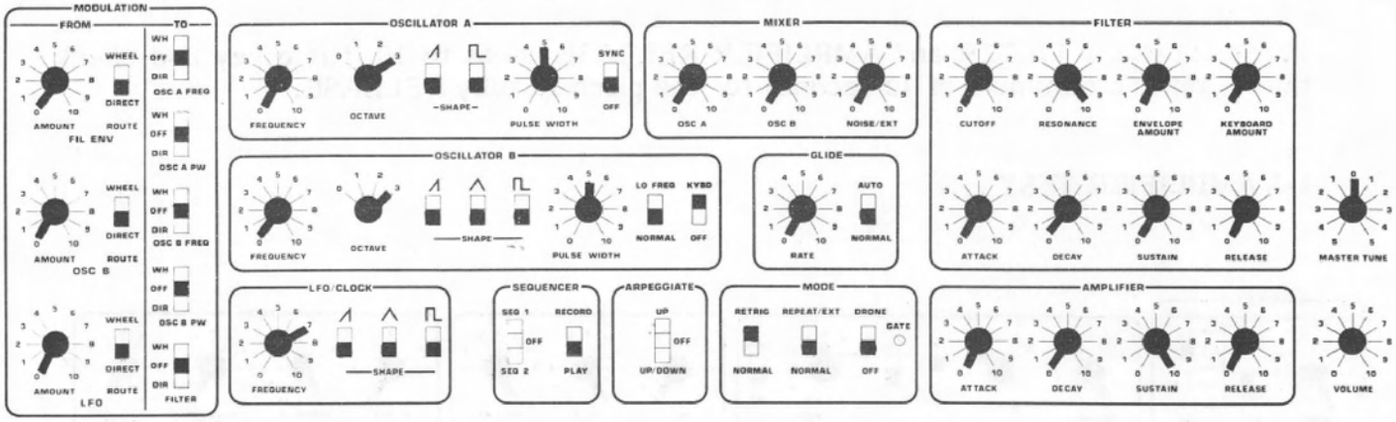


Figure 1-5
FILTER TEST PATCH

1. Patch according to Figure 1-5. NOTE: Unless you play staccato or switch to RETRIG mode, the envelope generator will not retrigger

2. Rotate FILTER CUTOFF knob 0 - 10, listening for sine-wave oscillation. The superaudio range is encountered at about 7 on the dial.

3. Set FILTER CUTOFF to 3. Raise FILTER KEYBOARD AMOUNT. As this knob is advanced, the notes heard will approach the diatonic scale tones. With KEYBOARD AMOUNT set to 8, the scale should be fairly accurate. Leave knob set to 8.

4. Hold a key and rotate FILTER ENVELOPE AMOUNT 0 - 10. This should not detune the pitch. If it does detune the filter, look into the Filter Envelope Generator circuit for the source of the offset. It is normal to hear an increasing transient as you advance ENVELOPE AMOUNT. This is the voltage peak between the ATTACK and DECAY periods--which becomes audible because the Envelope Generator is being triggered. Although the knobs are set to 0, it still takes a finite time to cycle through the ATTACK and DECAY periods. Leave knob set to 2.

5. Decrease FILTER RESONANCE to the point where oscillation stops and note dial indication. It should be between 5 and 6. Return knob to 10.

6. Increase FILTER ATTACK knob to 6. This should give about 1-sec attack time, as indicated by the pitch which gradually rises then "snaps back" to its starting pitch. Return to 0.

7. Increase FILTER DECAY knob to 6. This should give about 1-sec decay time. Return knob to 0.

8. Rotate FILTER SUSTAIN knob 0 - 10. It should smoothly increase filter frequency. Leave knob set to 10.

9. The next step requires increasing the AMPLIFIER RELEASE time so you can hear the FILTER RELEASE time. Start with AMPLIFIER RELEASE set to about 8. Set FILTER RELEASE knob to 6. This should give about a 1-sec release time.

10. Set both the FILTER and AMPLIFIER RELEASE knobs to 10. Hit a key and check that it takes a minimum of 15 seconds for the pitch to fully RELEASE.

1-8 AMPLIFIER TEST

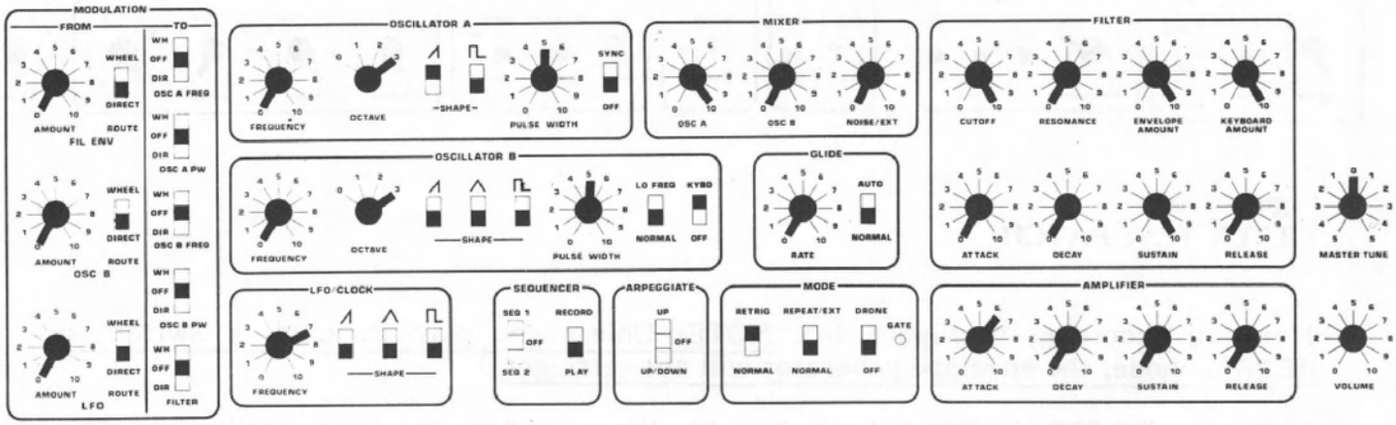


Figure 1-6
AMPLIFIER TEST PATCH

1. Patch according to Figure 1-6.

2. With AMPLIFIER ATTACK set to 6, the attack time should be about 1 second, heard as a rising volume which then "snaps back" to silence. Return knob to 0.

3. Increase AMPLIFER DECAY knob to 6. This should give about 1-sec decay time. Return knob to 0.

4. Rotate AMPLIFER SUSTAIN knob 0 - 10. It should smoothly increase amplitude. Leave knob set to 10.

5. Increase AMPLIFER RELEASE knob to 6. This should give about a 1-sec release time.

6. Set the AMPLIFIER RELEASE knob to 10. Hit a key and check that it takes a minimum of 15 seconds for the note to fully RELEASE.

1-9 MODULATION TEST

This test checks the LFO waveshapes, the three MODULATION FROM AMOUNT knobs and ROUTE switches, and the five destination (TO) switches. (The FIL ENV and OSC B modulation sources were tested above.) Since this test includes the LFO, don't use the arpeggiator or sequencer.

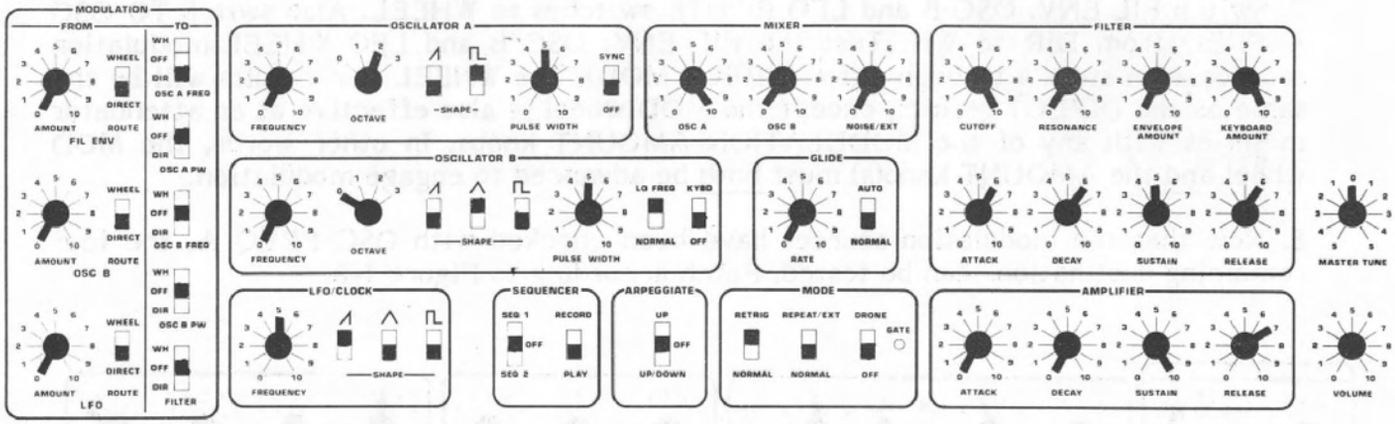


Figure 1-7
MODULATION SOURCE TEST PATCH

1. Patch according to Figure 1-7. (AMPLIFIER RELEASE must be greater than FILTER RELEASE to hear the complete filter envelope.)

2. Hold a key or use DRONE. Raise the LFO AMOUNT knob and note increasing frequency sweep of OSC A. Since OSC A frequency is being controlled by the LFO sawtooth, the frequency rises consistently, then snaps back to the "initial" frequency (para. 2-19).

3. Switch LFO SAWTOOTH off and LFO SQUARE on. This will give a "trill" effect, with the interval expanding with increased LFO AMOUNT. At 4 - 5 on the dial the higher note will be an octave above the initial frequency. At about position 8 the range will be two octaves. (para. 2-19)

4. Switch LFO SQUARE off and LFO TRIANGLE on. A symmetrical vibrato should be heard. Adjust LFO FREQUENCY 0 - 10 to explore the range of vibrato available (which is from about 1/4 to about 25 Hz). Leave LFO FREQUENCY set to about 6. Return LFO AMOUNT to 0.

5. Adjust OSC B AMOUNT 0 - 10 to check OSC B as modulation source. The effect will be a vibrato similar to that produced by the LFO. Adjust OSC B FREQUENCY to hear the range. Leave OSC B FREQUENCY and OSC B AMOUNT set to 0.

6. If used, switch DRONE OFF. Play slowly while adjusting MOD FIL ENV AMOUNT knob 0 - 10 to check the filter envelope as modulation source. The filter envelope has been patched in Figure 1-7 with 1-sec ATTACK, DECAY, and RELEASE times. Applying this envelope to OSC A FREQ gives a frequency sweep which rises for 1-sec, decays at the same rate to the sustain level while the key is held, then releases to the initial frequency at the same rate when the key is released. The range of the sweep is increased as you advance the FIL ENV AMOUNT knob. Return FIL ENV AMT to 0.

7. Switch FIL ENV. OSC B and LFO ROUTE switches to WHEEL. Also switch TO OSC A FREQ from DIR to WH. Test the FIL ENV, OSC B and LFO WHEEL-modulation sources as in steps 4 through 6 (for DIRECT MOD). The WHEEL test results will be the same as the DIRECT results, except the MOD wheel is also effective as an attenuator in series with any of the MODULATION AMOUNT knobs. In other words, the MOD wheel and the AMOUNT knob(s) must both be advanced to engage modulation.

8. Now that the modulation sources have been checked with OSC FREQ A, the four remaining destinations can be tested. Patch according to Figure 1-8.

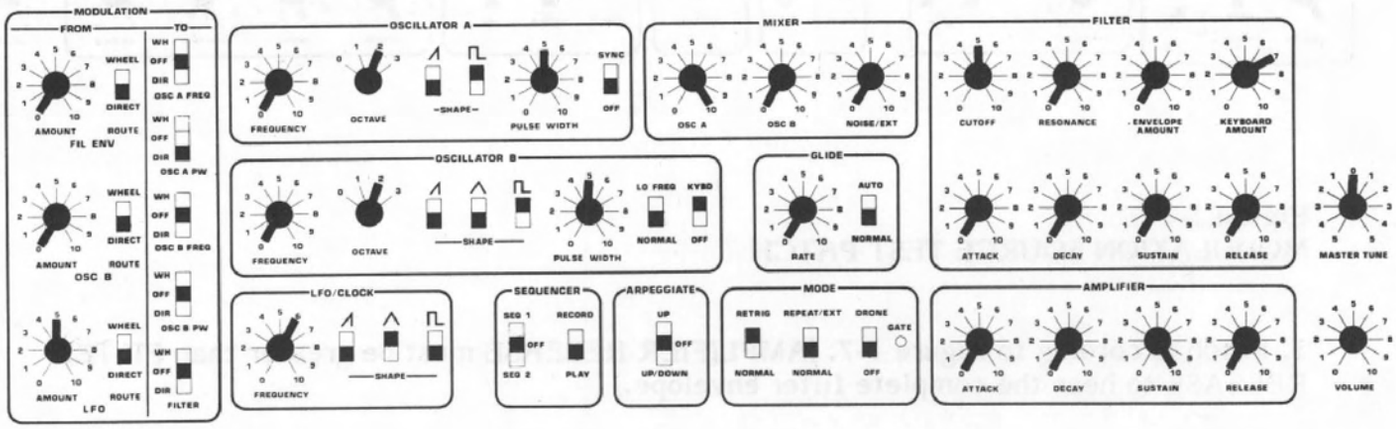


Figure 1-8
MODULATION DESTINATION TEST PATCH

9. Play and listen to pulse-width modulation of OSC A. Raise LFO AMOUNT to check depth of modulation. Set to 10, the LFO triangle peaks may cut-off OSC A PULSE (by forcing it to dc).

10. Switch TO OSC A PW off. Turn MIXER OSC A to 0. Turn MIXER OSC B to 10. Switch TO OSC B FREQ to DIR. This should create vibrato as heard in step 4, above. Check depth by adjusting LFO AMOUNT.

11. Switch TO OSC B FREQ off. Switch TO OSC B PW to DIR. This should produce pulse-width modulation as heard in step 9.

12. Switch TO OSC B PW off. Switch TO FILTER to DIR. The LFO should now modulate the filter cutoff frequency, giving a "wah-wah" effect.

13. Switch LFO ROUTE from DIRECT to WHEEL and repeat steps 8 - 12 except switch the destinations to WHEEL (instead of DIR) to test the WHEEL destination paths.

1-10 BACK PANEL TEST

1. If desired, connect electric piano, guitar, or microphone to AUDIO IN. Switch mode to EXT. Raise MIX NOISE/EXT knob and adjust for adequate gating by the external signal.

2. With a suitable patch, plug one end of a mono phone cable into J6 FILT CV IN. This should disable the FILTER KEYBOARD AMOUNT knob. Connect other end to CV OUT. Unit should play normally. Disconnect cable.

3. Plug one end of mono phone cable to J2 CV IN. This should disable the keyboard. Connect other end to CV OUT. Unit should play normally. Remove cable.

4. If a GATE source is available connect to GATE/CLK IN, and switch MODE to REPEAT/EXT check that the envelopes are gated and sequencer advanced with each pulse.

5. GATE OUT can be checked with a voltmeter. The output goes from 0 to +5V when a key is pressed.

1-11 TUNING FLOW CHART

Figure 1-9 on the next page is a flow chart for selectively checking Pro-One tuning. Especially because most tuning trimmers are accessible to the owner, whenever the Pro-One is grossly out of tune it is probably best to completely retune according to Section 5, below or in the the Operation Manual, CM100B. But often only a couple of trimmers may need "touching-up," in which case following the chart may save you significant time.

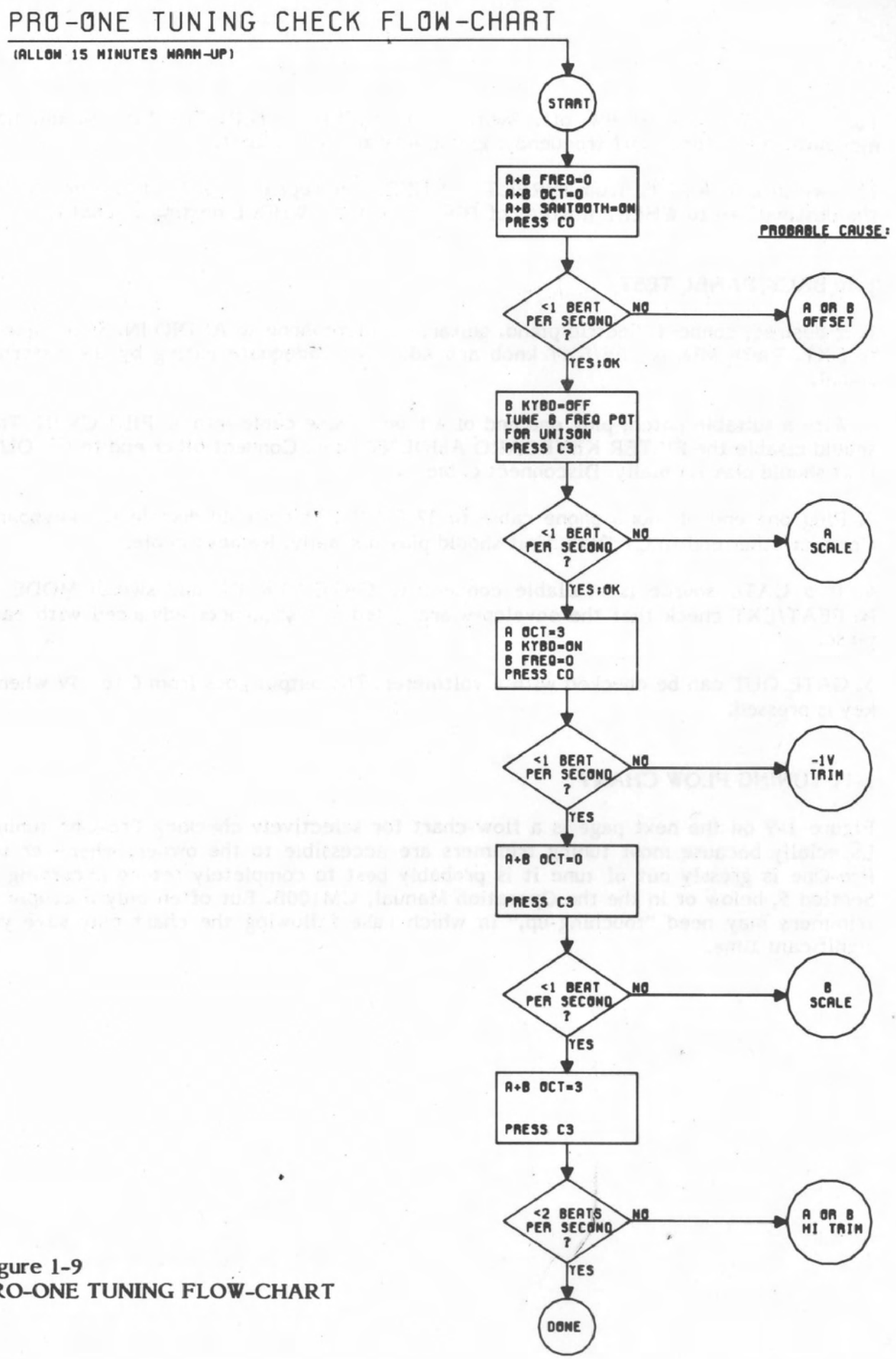


Figure 1-9
PRO-ONE TUNING FLOW-CHART

2-0 INTRODUCTION

This section explains the Pro-One's hardware theory of operation. The microcomputer program (software) is not generally discussed because it is proprietary and because the program details are usually not relevant to service problems. That is, you can't "fix" the software (you can replace it, by replacing the Microcomputer IC). Note that if you first understand the hardware surrounding the microcomputer, you will be able to deduce the basic program functions.

2-1 GENERAL

The Operation Manual CM100B covered general function and signal flow of the voice and modulation sections. The Pro-One is a monophonic synthesizer in which the analog voltage-controlled sound sources and modifiers are controlled by a microcomputerized keyboard, as shown in Figure 2-0.

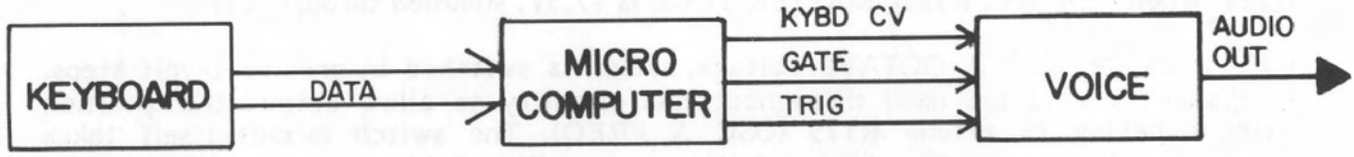


Figure 2-0
PRO-ONE GENERAL BLOCK DIAGRAM

The microcomputer generates the keyboard control voltage (KYBD CV), which is the main determinant of oscillator pitch, and the GATE and TRIGGER (TRIG) signals, which control the filter and amplifier envelope generators.

Figure 2-1 shows more functional detail. The integrated microcomputer contains a central processor unit (CPU), read-only memory (ROM), and random-access memory (RAM). The CPU follows the program in ROM by which it "reads" the keyboard, SEQUENCER, ARPEGGIATE, and MODE switches and forms the appropriate output signals. The CPU uses RAM to keep track of the keyboard and switch status and to store latched arpeggios and sequences.

To play a note the microcomputer first reads the keyboard to find out what key is pressed, then sends the key number in parallel, 6-bit binary form to the digital-to-analog converter (DAC). When it receives the DAC ENABLE (EN) signal, the DAC converts the key number to the analog KYBD CV for OSC A, OSC B, and the FILTER. The Microcomputer then issues the TRIG and GATE signals which enable the Filter and Amplifier Envelope Generators. The TRIG only appears briefly when the key is first struck. When the key is released, the GATE goes off, initiating the RELEASE period(s).

For the remainder of this section, please refer to Figure 2-2, Abstract Schematic, and the Interconnect Diagram and Schematics (SD121/SD112) in Section 3.

2-2 OSCILLATOR A

The Pro-One's three oscillators (OSC A, OSC B, LFO) use the CEM 3340 integrated voltage-controlled oscillator (VCO). As in the Prophets and most standard synthesizer modules, these VCOs operate in exponential mode (as opposed to linear mode), scaled at 1V/octave. This means a CV change of exactly 1V ideally produces a pitch change of exactly one octave, i. e. a doubling of frequency. The basic range of OSC A (and OSC B) is seven octaves, resulting from up to 3V provided by the keyboard, up to 3V provided by the OCTAVE switch, and up to a little more than 1V provided by the FREQUENCY knob.

The VCO itself is of course a complex of other circuits. Basically, the summed CV input drives an exponential control current generator, which charges the external timing capacitor. The increasing positive charge produces the ascending portion of a triangle wave (by direct integration). When this charge reaches a specific level, a comparator switches- in a discharge path for the capacitor, producing the descending portion of the triangle wave. The sawtooth is obtained from the triangle via another comparator and switch. The pulse is created by a comparator which toggles as the sawtooth level matches the pulse width CV input.

See SD112. Looking at the various signals summed into U102 OSC A's control pin 15, R123 sets the initial frequency. R119 OSC A FREQUENCY knob provides over 1V of control through R131. R120 OSC A OFFSET trimmer adjusts initial frequency through R124. When centered, R1210 MASTER TUNE is +7.5V, summed through R126.

R133 adds the OSC A OCTAVE voltage, which is switched in precise 1-volt steps. Precision resistors are used throughout this circuitry to allow octave transposition without having to retune R119 (OSC A FREQ). The switch circuit itself takes advantage of the summing ability of the op amp. The divider containing R1111 -1V trimmer, R1110, and R1109 places -1V on the input of Buffer U107-7. Figure 2-3 shows the function of S105 OSC A OCTAVE switch, which can also be thought of as a 2-bit DAC. The low-impedance voltage source is switched through R-2R summing resistors to an inverting summer, becoming a positive voltage at U104-14. R167, of course, sets the gain to 1. C117 makes a low-pass filter to suppress switching noise.

Summed through R127, R1 PITCH wheel contributes a nominal 0V when centered. D101 and D102 form a "deadband" circuit. The inherent diode voltage drop reduces the requirement that the PITCH wheel be exactly centered to not detune the oscillators. The wiper can be between +/- 700 mV before the oscillators are affected.

OSC A is always under control of the KYBD CV through R121, which is precision-matched to R133 OSC A OCTAVE summing resistor. (The origin of the KYBD CV is discussed in para. 2-12.)

S104 MODULATION TO OSC A FREQ switch applies a modulation CV, mixed over either the WHEEL (WH) or DIRECT (DIR) modulation busses, through R125. (The Modulation source circuitry is discussed in para. 2-8.)

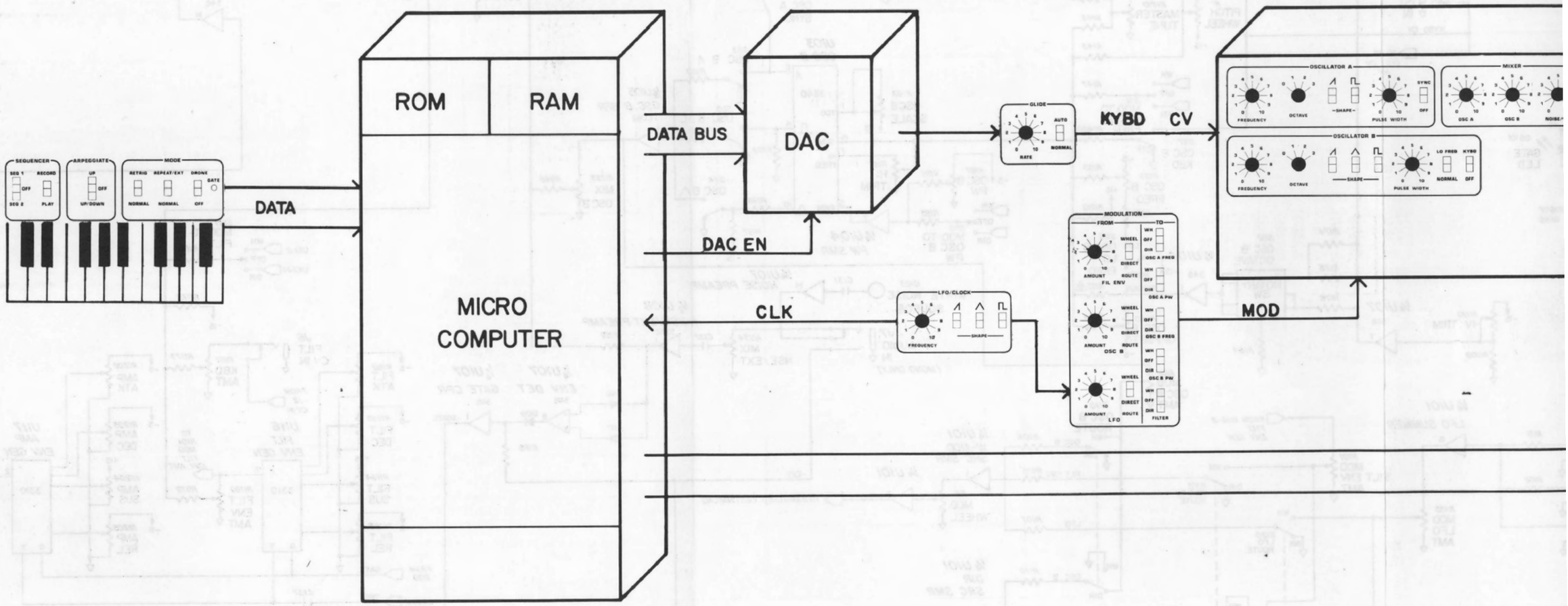
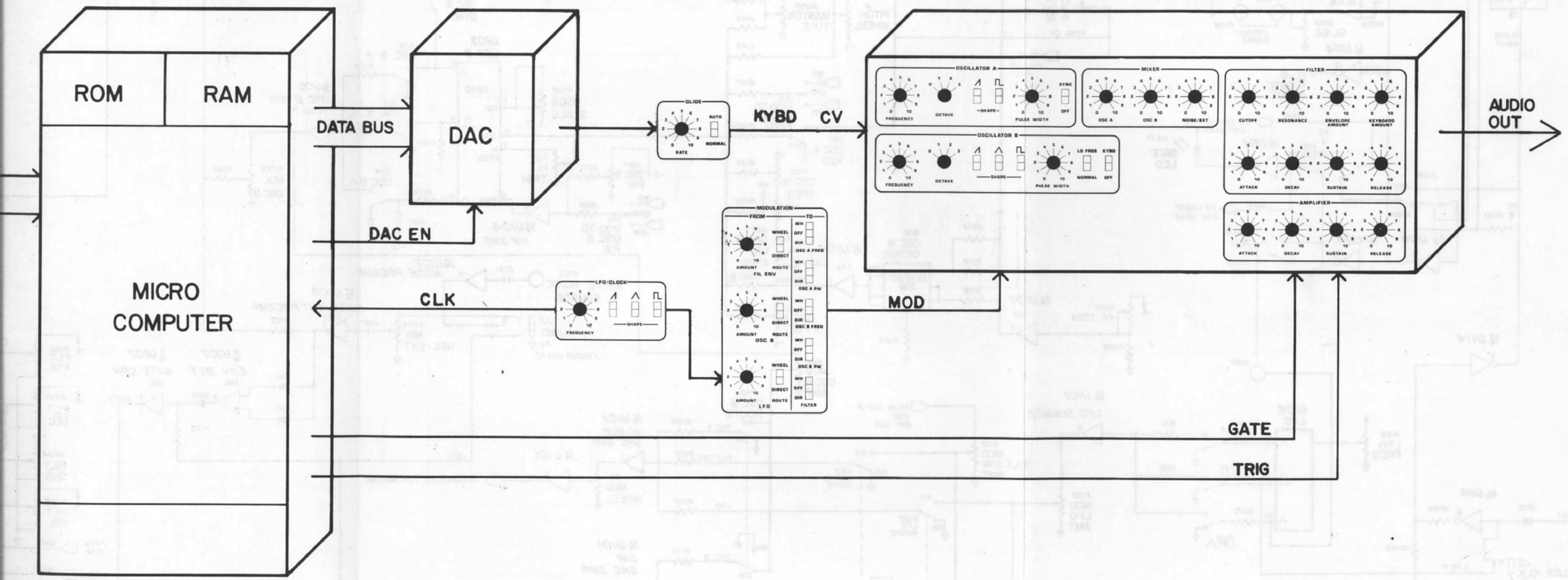


Figure 2-1
PRO-ONE FUNCTIONAL BLOCK DIAGRAM


ROM
RAM
MICRO COMPUTER
DATA BUS
DAC
DAC EN
CLK
GLIDE
RATE
AUTO
NORMAL
KYBD CV
MODULATION
FROM
TO
WHEEL
DIRECT
AMOUNT
ROUTE
FIL ENV
OSC B
LFO
WH
OFF
DIR
OSC A FREQ
OSC A PW
OSC B FREQ
OSC B PW
FILTER
LFO/CLOCK
FREQUENCY
SHAPE
MOD
OSCILLATOR A
FREQUENCY
OCTAVE
PULSE WIDTH
SYNC
OSCILLATOR B
LO FREQ
KYBD
NORMAL
MIXER
OSC A
OSC B
NOISE/EXT
FILTER
CUTOFF
RESONANCE
ENVELOPE AMOUNT
KEYBOARD AMOUNT
ATTACK
DECAY
SUSTAIN
RELEASE
AMPLIFIER
AUDIO OUT
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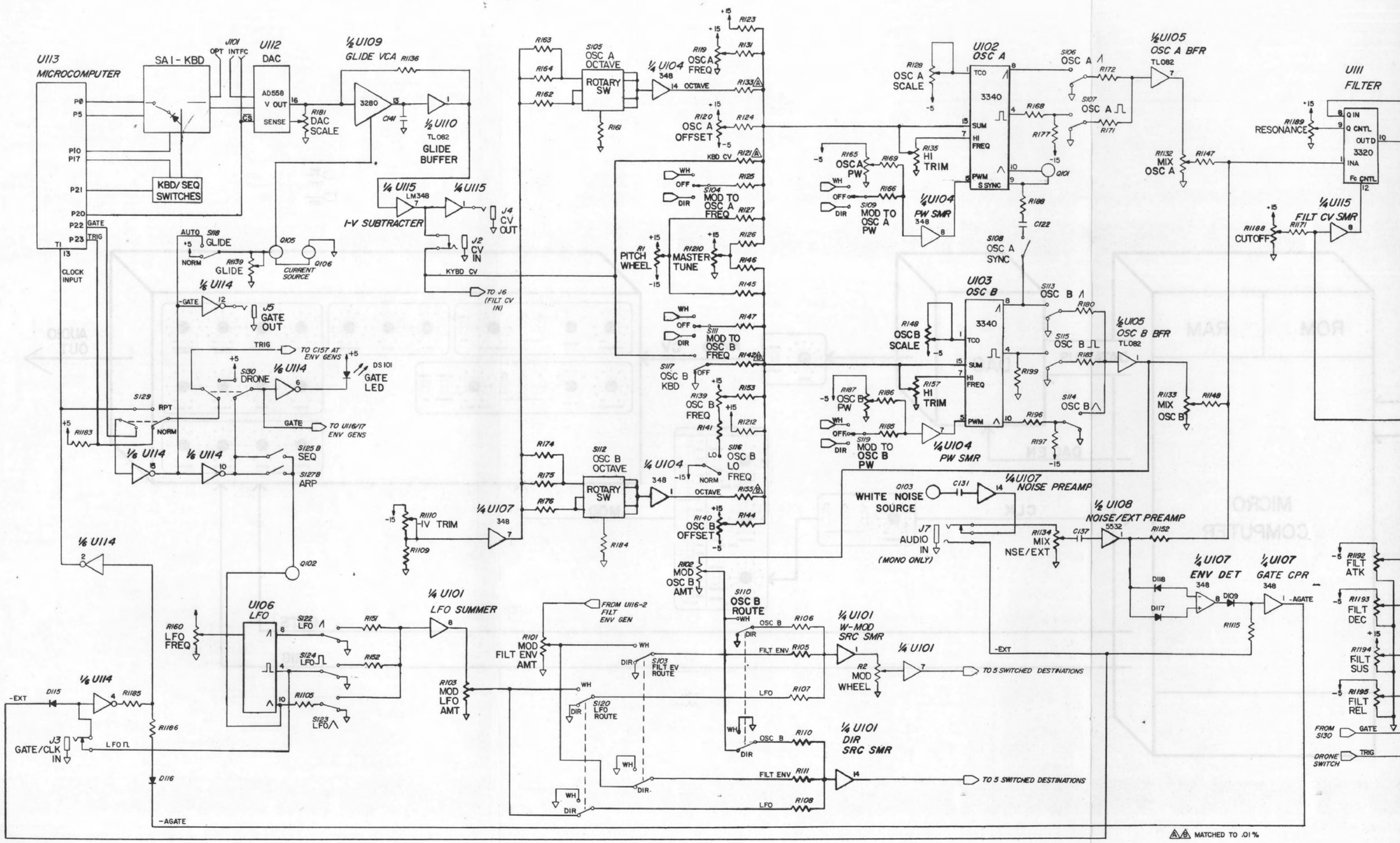


Figure 2-2
PRO-ONE ABST

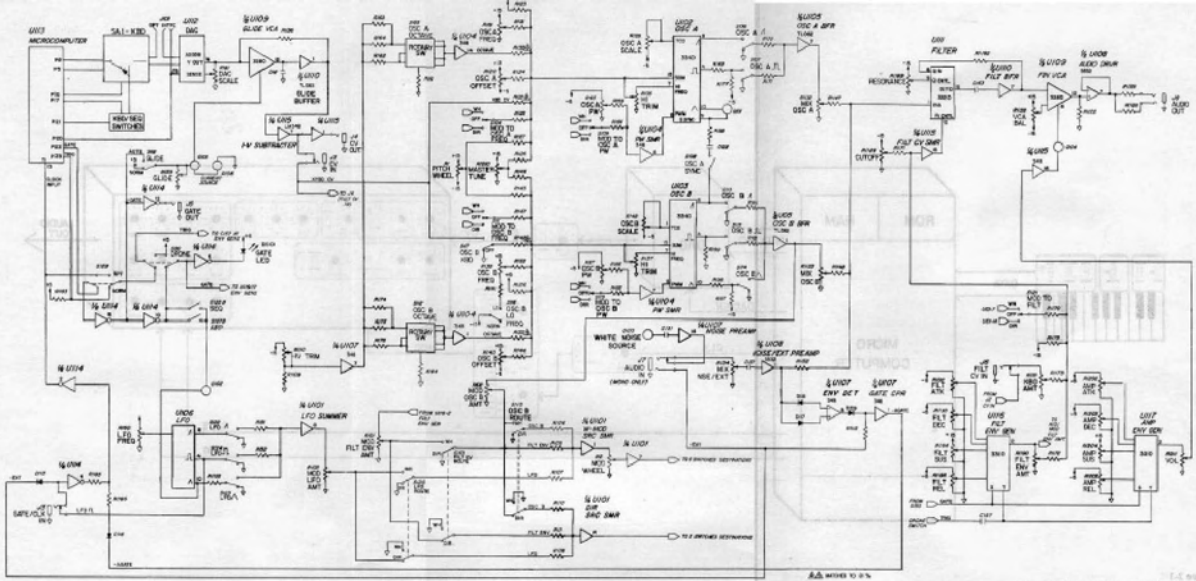


Figure 2-2
PRO-ONE ABSTRACT SCHEMATIC

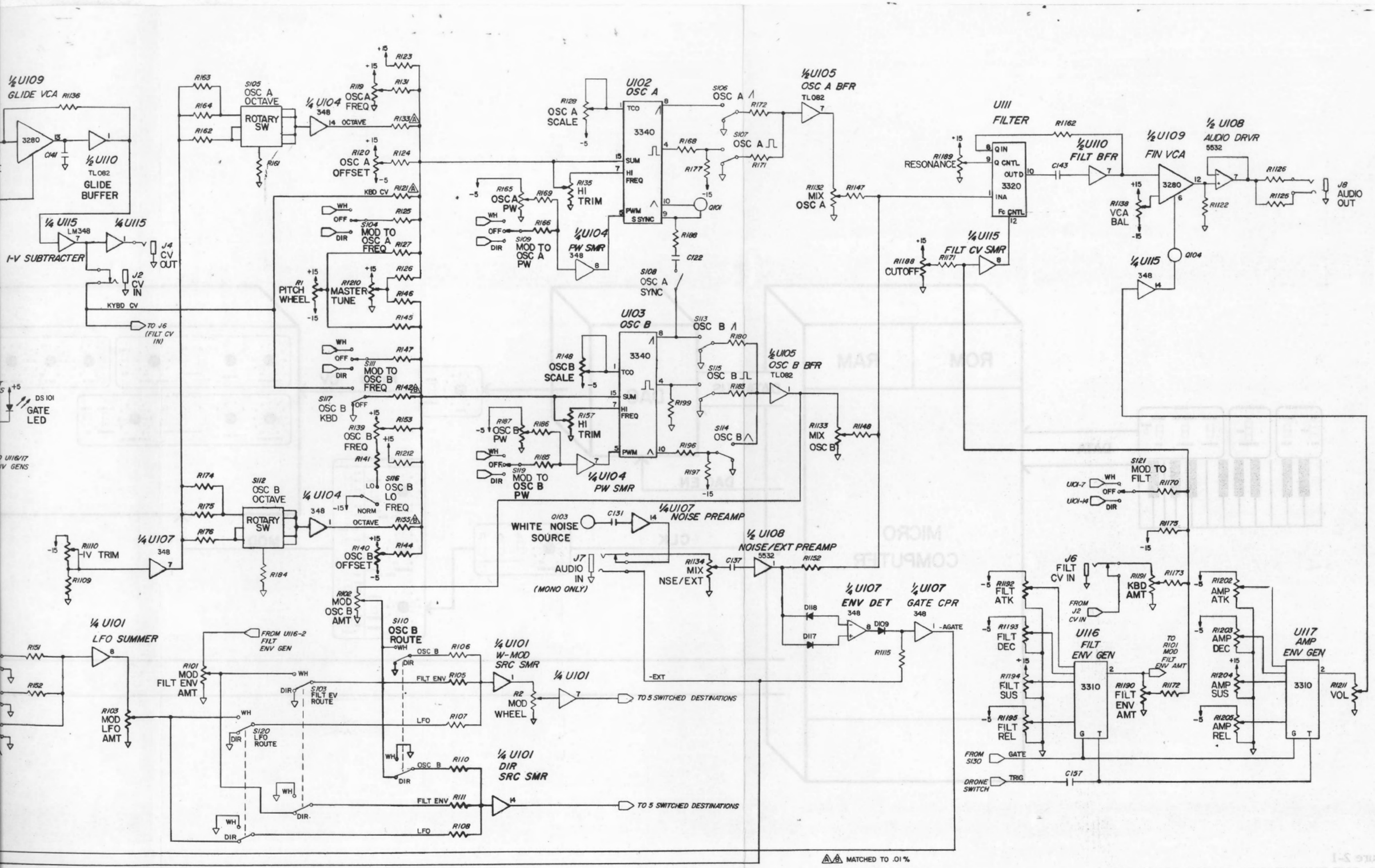


Figure 2-2
PRO-ONE ABSTRACT SCHEMATIC

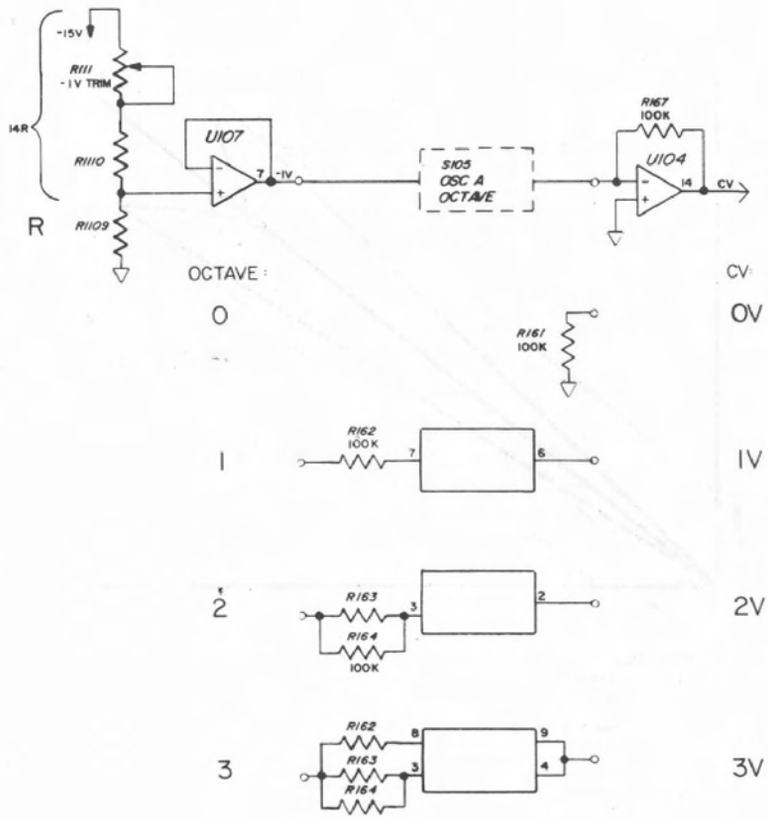


Figure 2-3
OSC A OCTAVE SWITCH

Pitch accuracy amid varying temperatures is the main challenge of VCO design. As it heats and cools, the exponential control current generator charges the timing capacitor more or less quickly, altering the oscillation period (pitch). The outstanding stability of the Pro-One's oscillators results from the inclusion in the 3340 of a temperature compensation (TEMPCO) circuit which has the same temperature characteristics as the exponential generator, but which adjusts the effective CV to counteract drift in the exponential generator. This adjustment takes place in the precision multiplier.

R128 adjusts OSC A SCALE by determining the current gain of the precision multiplier through the temperature compensation (TCO) circuitry. R122 and C103 compensate the precision multiplier. R134 (at pin 14) converts the current output of the precision multiplier into a drive voltage for the 3340's exponential current generator. R137 (at pin 13) sets the reference current for the generator. R136/C106 compensate the generator. C105 (pin 11) is the timing capacitor which is the main determininant of oscillator frequency range. It is a polysterene type for low leakage and best stability.

R132 feeds-back a high-frequency tracking correction voltage output from pin 7 which is trimmed by R135 OSC A HI TRIM to sharpen the oscillator in compensation for an inherent high-end flatness resulting from error in the exponential generator.

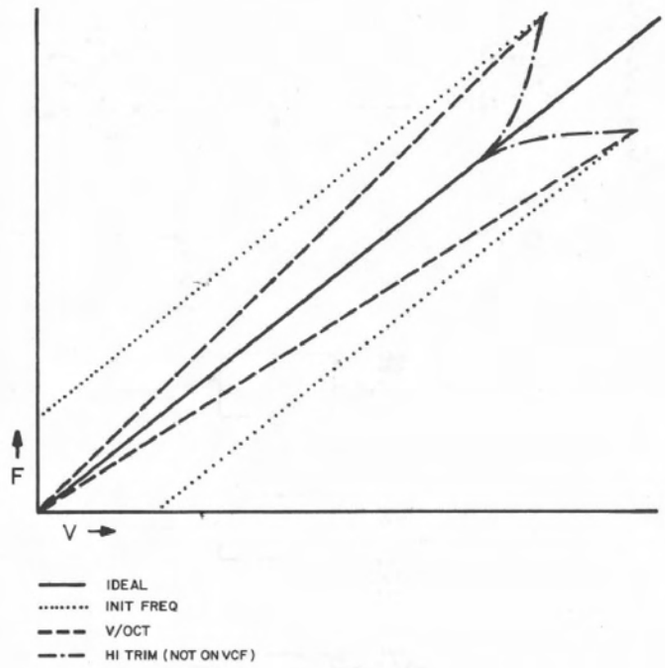


Figure 2-4
VOLTAGE-CONTROL TRIMS

Figure 2-4 graphs the ideal VCO function and the corrections possible with the trimmers provided. As can be seen, there is considerable overlap between the adjustments. (Thus, tuning procedures are written specifically to overcome these interactions.) Initial frequency, or OFFSET, raises or lowers the function. V/OCT adjusts the slope of the line, and HI TRIM adjusts the function above about 3 kHz.

OSC A's SAWTOOTH output at pin 8 ranges 0 - 10V. It is switched by S106 through summing resistor R172 to summer U105-7. The PULSE output from pin 4 is pulled down by R177, and is attenuated (with respect to the sawtooth) by R171.

CVs for OSC A pulse-width modulation are summed and inverted by U104-8 yielding a basic control range of 0 to +5V into U102-5. R165 OSC A PULSE WIDTH knob connects through R169. S109 MOD TO OSC A PW selects the modulation buss summed through R166. R170 sets the summer gain to 1. C118 filters noise which may be generated by rotating R165.

U102-9, S SYNC is a 5-V source which biases the base of Q101 through R138. C108 is simply a dc filter. When closed, S108 OSC A SYNC couples the falling edge of the OSC B sawtooth through C122 and R188, which turns on Q101. The internal sawtooth buffer connected to U102-10 is thus pulled-down to -5V, resetting it. This "hard syncs" OSC A to B, independently of whatever OSC B waveforms are switched on.

Further details of the CEM 3340 can be found in the Appendix.

2-3 OSCILLATOR B

OSC B is similar to OSC A except that besides being a pitch source it can be a modulation source and can therefore operate as an LFO with or without keyboard control. Only the differences between OSC B and OSC A will be mentioned. S116 LO FREQ switch extends the range of R139 OSC B FREQUENCY knob by connection to -15V. The KYBD CV path through R142 contains S117 for disabling keyboard tracking.

The unused S SYNC input is bypassed by C115 to prevent synchronization to noise.

OSC B's output circuitry differs from OSC A by having the SAWTOOTH and PULSE outputs amplified by differential buffer U105-1 with a gain of 1. For the TRIANGLE output, R197 contributes enough negative dc voltage to pull the triangle level down to be symmetrical about ground level (rather than positive-going) so as to not offset modulation destinations. Figure 2-5 shows how the waveforms normally add together.

Besides driving R1133 MIX OSC B knob, the OSC B output is tapped for the MODULATION circuitry, discussed below.

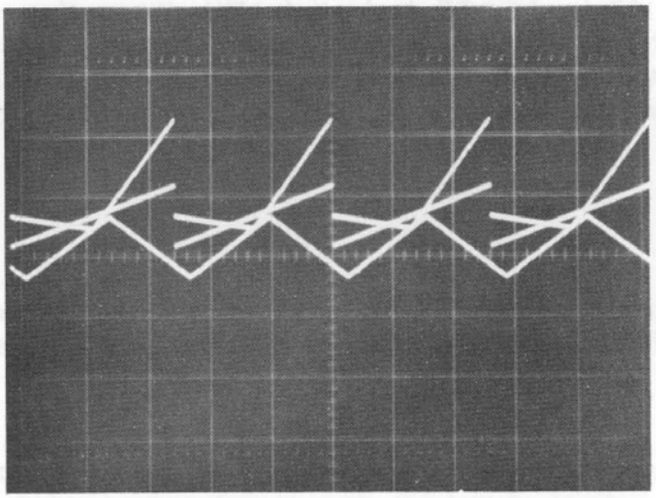


Figure 2-5
OSCILLATOR B SAWTOOTH and TRIANGLE OUTPUT

2-4 MIXER/NOISE/EXTERNAL

The mixer knobs are simply attenuators which set the level of selected OSC A (R1132), OSC B (R1133) waveforms and NOISE (R1134) sent to the filter. R1147 and R1148 sum the adjusted oscillator outputs into the filter.

The white noise source is created by reverse-biasing the emitter-base junction of PNP Q103 far above its breakdown threshold. (To increase the noise output with certain later batches of transistors, R1120 was changed from 100K to 200K.) C131 ac-couples the resulting noise to non-inverting amp U107-14, which has a gain of 3 (1+R1116/-R1117).

NOISE/EXT input switching is accomplished by J7, which is a "stereo" jack wired for "mono" use. With no plug inserted, noise connects through the "tip" switch contact to R1134 MIXER NOISE/EXT knob. Connecting an external mono phone plug to J7 AUDIO IN bypasses the noise with the external audio, and also grounds the sleeve contact on the jack. This creates the active-low -EXT signal which enables the gate select logic and audio gate comparator (both discussed below).

U108-1 Noise/Ext Preamp is an ac-coupled non-inverting microphone-type preamplifier with a frequency roll-off just above 20 kHz. R1152 sums its output into the filter.

The Preamp also drives U107-8 Envelope Follower, which rectifies the external audio amplitude from 0 to +15 Vdc, and also drives U107-1 Audio Gate (AGATE) Comparator (CPR). With no audio input, U107-1 -AGATE is high (+15V). When the rectified envelope across R1115 exceeds the threshold set by divider R1112 and R1114 (with -EXT grounded), -AGATE goes low. The application of the -AGATE signal is discussed below. To prevent oscillation around the threshold point, C130 briefly retains the peak voltage.

2-5 FILTER

The Pro-One's low-pass filter is based on the CEM 3320 integrated voltage-controlled filter (VCF). The control scale for its cutoff frequency matches the VCO scale of 1V/OCT.

There are many sources of filter cutoff CV into U111-12. Working back from U115-8 inverting FILTER CV SUMMER, R1188 CUTOFF knob is summed through R1171. S121 MODULATION TO FILTER selects the modulation buss summed through R1170. R1173 sums the adjusted output of R1191 FILTER KEYBOARD AMOUNT knob, which is normally the keyboard voltage connected through J6 FILTER CV IN. J6, of course, allows for external filter control independently of the keyboard. (When troubleshooting for "no filter keyboard voltage," check the contacts on this jack.) R1172 connects the FILTER ENVELOPE GENERATOR output from U116-2, adjusted by R1190 FILTER ENVELOPE AMOUNT. (Note that it is redundant to route the filter envelope both through R1190 and through S121. See below, under MODULATION SOURCES.) Finally, R1175 sets the basic control range.

The filter output, U111-10 is ac-coupled by C143 to non-inverting buffer U110-7, which has a gain of 2.4 (R1144/R1146). This buffer drives both the Final VCA stage and, through divider R1162/R1163, the "resonance gain cell" internal to the 3320, which actually feeds filter output back to the input of stage A. The gain of this internal amp is adjusted by R1189 FILTER RESONANCE knob through R1157.

Details of the 3320 and associated components can be found on its Data Sheet in the Appendix.

2-6 FINAL VCA

The Final VCA U109-12 uses 1/2 of the RCA CA3280 dual operational transconductance amplifier (OTA). (The other 1/2 is used in the Glide Circuit, see para. 2-13) The OTA is similar to the typical op amp in input and open-loop gain characteristics but the output is current rather than voltage. The magnitude of the output current is equal to the product of the transconductance (rather than the voltage gain) and the input voltage. The transconductance is adjusted by the amplifier bias current (Iabc) at pin 6 (see Appendix). A second terminal (Id) for biasing linearizing input diodes, controls the transfer characteristic as shown on the Data Sheet (See Appendix--Figure 12). R1141 sets Id, which determines the input impedance of the OTA. As Id increases, the effective resistance between pins 9 and 10 decreases.

Since the 3280 is controlled by current, the term CV is not really accurate. The 3280 "CV" from the Amplifier Envelope Generator is converted to a control current (CC) by Q104, 2N4250 PNP transistor. R1143 limits the amount of current which can be developed.

R1138 VCA BALANCE trimmer cancels OTA offset, ensuring that even with maximum Iabc, there is no output voltage in the absence of an input signal. R1122 develops suitable drive voltage from the OTA's current output.

U108-7 5532 voltage follower can drive 600-Ohm loads, so is not bothered when R1125 is grounded by a mono plug connected to J8.

2-7 ENVELOPE GENERATORS

U116 Filter and U117 Amplifier Envelope Generators are based on the CEM 3310 IC. Its output is 0 to +5 Vdc changing over the time periods set by the input timing CVs. When applied to the VCF and FINAL VCA, the transient voltage determines the frequency and amplitude contours of the voice.

The circuitry around both generators is minimal. The knobs simply set the desired control voltages. Note that the ATTACK, DECAY, RELEASE timing controls are all wired from -5V to ground, while SUSTAIN is wired from ground to +15V.

If it is desired to extend the maximum ATTACK or RELEASE periods, decrease the 1.8M resistors (e.g. R1196, R1200, R1206, R1205) to 1.6M, which will extend the range to 20 seconds. (Note: such modifications may conflict with published patch diagrams.)

The TRIGGER and GATE signals are generated by circuitry discussed below. C157 forms the needed pulse for the trigger.

R1211 adjusts VOLUME by attenuating the CV to the FINAL VCA. R1168 contributes a negative voltage to the inverting input of U114-14, creating a positive offset required to compensate for the drop across the current-converting transistor Q104 and R1143.

Details of the 3310 and associated components can be found on its Data Sheeet the Appendix.

2-8 MODULATION SOURCES

The five modulation destinations were discussed above. The modulation source circuitry is straightforward. See SD121. Each source (LFO, FILT ENV, and OSC B) has an attenuator and DPDT switch. Each switch simultaneously connects a source to one modulation buss while grounding the input to the other modulation buss. For example, in the position shown, S120 routes LFO from R103 to R108 and U101-12, the Direct Source Buffer input. This buffer has a gain of 2. At the same time, S120 grounds R107 to U101-3, the W-MOD Source Summer input. U101-1 also amplifies the mixed modulation CV by about 6, before supplying it to R2 MOD WHEEL. U101-7 buffers the MOD WHEEL output.

As mentioned above, it is redundant to use the filter envelope through both R1190 FILTER ENVELOPE AMOUNT knob and R101 MODULATION FILT ENV AMT to S121. The path is intended for Filter Envelope Modulation of OSC A or B FREQ or PW.

2-9 LFO

U106 LFO is a CEM 3340, like OSC A and B. Its only variable CV is from R160 LFO FREQUENCY through R191. Divider R1108/R1107 at pin 5 fixes the pulse width at 50%, giving a square wave, whose edge is sharpened by feedback through R1106. The LFO output circuit is similar to OSC B.

2-10 MICROCOMPUTER

We now turn to the Pro-One's digital circuitry, of which the Intel 8021 single-chip Microcomputer is the chief component. The 8021 contains 1K x 8 bits of ROM which is mask-programmed with instructions, and 64 x 8 bits of dynamic RAM. L101 controls the 8021's internal clock circuit, establishing a frequency of about 3 MHz.

When power is first turned on, U113-17 RESET is pulled high by C153. The positive-going pulse clears the internal registers and sets the program counter to 0. D114 discharges C153 on power off.

All input to the microcomputer results from switch closures either from the keyboard, or the mode controls. The keyboard is merely a bank of switches which the computer scans in fundamentally the same way it would scan a calculator keyboard. Each key has a corresponding memory bit which is set (1) or reset (0) if the key is on or off. This is how sequences can be remembered and the arpeggiator latched. The key closures are processed into a single binary number sent to the DAC. The changing keyboard "status" also produces the TRIG and GATE signals which articulate the voice. The remaining switches activate different areas of the microcomputer program, resulting in a change of modes.

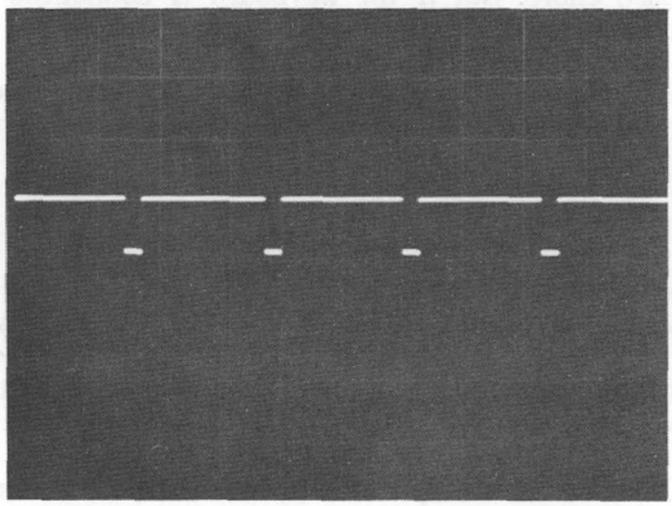
The computer peripheral interface lines are configured as a data driver (P00-P05) which sends 5 bits of data to the matrix "rows" and 6 bits to the DAC, an 8-bit data receiver (P10-P17) for the switch matrix "columns", plus output lines which refresh the DAC (P20), activate the control switches (P21), and output the GATE (P22) and TRIGGER (P23) signals to the voice.

The T1 input at pin 13 accepts clock signals which may arise from the LFO, an external gate source, or an external audio source (-AGATE).

2-11 KEYBOARD/SWITCH MATRIX

Looking at the keyboard matrix more closely, the basic scanning operation is to activate one matrix row of contacts on eight consecutive keys, then check the intercepting columns for the presence of a bit. The resulting data uniquely identifes a combination of switch closures in each row. The group of five bytes which represent the five scanned matrix rows form a "map" in RAM. By comparing two such maps made in successive "scans," the computer detects what key(s) are being pressed and released and decides whether to refresh the DAC with a new key number and output the TRIGGER and GATE.

Actually the matrix harware works on negative logic. To check the first row, U113 outputs the number 1 1110 (1EH) on the data driver. This means pins 5 through 8 are high, while pin 4 (P00) pulls the first row low. The receiver inputs (P10-17) are being pulled high by internal pull-up resistors. So if no keys in the first row are held, the receiver inputs the number 1111 1111 (FFH). But suppose key D0 is held. This pulls receiver line P12 low, so the input number would be 1111 1011 (FBH). Figure 2-6 shows this signal.



U113-20 (P12)
D0 HELD
H=5 ms/div
V=5V/div

Figure 2-6
KEYBOARD RECEIVER LINE

Any single key or combination of key closures can be uniquely identified by these codes. To set up the second matrix row, the driver outputs 1 1101 (1DH) and again inputs the receiver data to check for key closures. This is repeated for the remaining lines. At the conclusion of the scan, the CPU "knows" what keys are being held. Normally, it then finds the number of the lowest key (for example D0 is 3), transposes it up an octave by adding 12 to it, and saves this number to send to the DAC.

The MODE, ARPEGGIATE, and SEQUENCER switches connected to P21 are scanned in the same way. The diodes wired throughout the matrix allow n-key rollover, which is the simultaneous pressing of any number of switches and keys. They prevent switched bits from returning through other closed switches on the same column, which would activate other rows in addition to the one the CPU thinks it is scanning.

If it is desired to change the ARPEGGIATE UP/DOWN function to DOWN only, add D103.

When troubleshooting the keyboard, check schematic for connections between problem keys. "Dead" notes, if not caused by broken J-wires or oxidation, usually occur in groups which belong to the same matrix row or column.

As you can see, all that is in the keyboard circuitry are the few keyboard control switches, some diodes, and U113 Microcomputer. Occasionally, physical shock can disconnect the keyboard cable. But if the keyboard is connected correctly and still doesn't work, it is a good bet to replace the Microcomputer.

If the GATE is stuck on, the problem could be a stuck key (but check also the DRONE switch). The easiest way to check for a stuck key is to disconnect the keyboard cable. The GATE should go off.

2-12 DAC

U112 DAC is an Analog Devices AD558 8-bit unit, but for best accuracy only the most-significant 6 bits are used. By no accident, the DAC is scaled to provide the exact voltages which the VCOs and VCF require to play semitones, which is 83 mV (1/12V)/step. If given the number 01, the DAC output is 83 mV (1/12V), if given the number 1101 (decimal 13), the output is 1.083V (13/12V), and so on.

As mentioned above, the actual binary numbers sent to the DAC are the key numbers (1 through 37) plus 12 units. This pre-addition allows the sequencer transpose function. Since the data bus cannot "go negative," it would only be possible to transpose-down the lowest octave recorded by subtracting (up to twelve units) from the recorded key number. This means the untransposed 3-V CV range from the DAC normally ranges from 1 to 4V. Thus when a maximum downward transposition is required, the DAC output will be 0 to 3V. On the other hand, maximum upward transposition will raise the output range from 2 to 5V.

The DAC has its own internal latch which is clocked by the positive-going DAC EN pulse from U113-26 (P20). Since, as mentioned above, the data driver outputs a series of different numbers when scanning the keyboard, the DAC EN signal is needed to tell the DAC when data output is specifically intended for it (rather than for the matrix). The CPU only refreshes the DAC when the CV is to change. (In other words, when a note is repeated the DAC is not refreshed.) To refresh, the microcomputer briefly pulls DAC EN low. The DAC latches the data on the rising edge of this pulse. R1181 DAC SCALE provides adjustment by altering the gain of the DAC's internal amplifier.

J101 Digital Interface connector provides access to the DAC input latch and the necessary control signals. Instructions for using the interface are in the Operation Manual. Briefly, U113 must be removed, R1182 added, and a jumper installed between U113-2, and J101-7. The external system then connects to J101. (For details, see Section 5.)

Ignoring the Glide circuit for the moment, U115-7 and associated resistors form a 1-V Subtracter converting the normal DAC range down to a conventional output range. U115-1 buffers the KYBD CV sent to J4 CV OUT. The KYBD CV sent to the oscillators and filters can be bypassed by an external input at J2.

2-13 GLIDE

The Glide circuit processes the KYBD CV from the DAC, causing it to slew between its discrete 83-mV steps. U109-13 OTA is the central component of the Glide circuit, which also contains current source Q105/Q106 and buffer U110-1. The buffered output from the voltage follower is fed back to the OTA input through R1136 so positive or negative current will flow into C141 if there is a difference between the feedback voltage and the input voltage through R1135. D110/111 protect the OTA inputs.

Divider R1167/R1166/R1165 is the Glide voltage source. When R1139 GLIDE RATE knob is set to 0 (ground), Iabc will be maximum because diode-connected voltage source Q106 forward-biases Q105's emitter 620 mV above ground. Transconductance will therefore be maximum, so plenty of current is available to charge C141 and the GLIDE output will follow the KYBD CV very closely. However as the GLIDE knob is raised, Iabc sourced by Q105 is inhibited, reducing the rate of charge to C141. It will thus take longer for the GLIDE output to approach KYBD CV. This creates a slew between the discrete voltage steps output by the DAC.

When S118 is switched to AUTO, C149 couples the -GATE signal (discussed below) which pulls-down the base of Q105, enabling collector current, thus disabling GLIDE. When -GATE goes high, D112 discharges C149 in preparation for the next -GATE.

2-14 GATE AND TRIGGER LOGIC

We've only left to inspect the miscellaneous circuitry which interfaces the internal or external clock sources and microcomputer. In normal modes, the GATE passes through S129 REPEAT/EXT, and is buffered by inverter U114-15. The resulting -GATE signal drives the Auto-Glide circuit, discussed above, and is re-inverted by U114-12 for J5 GATE OUT. U114-10 also re-inverts -GATE, producing the signal switched to the envelope generators by S130, and driving DS101 GATE LED, thorough U114-6.

R1183 speeds-up the rising edge of the TRIG signal. It is switched through S129 and S130. To trigger, the microcomputer momentarily pulls TRIG low. This pulse is coupled through C157 (see SD112) to the envelope generators.

Switching S130 DRONE on holds both the TRIGGER and GATE signals high. (Although the TRIG singal is ac-coupled to the envelope generators.

If S129 is switched to REPEAT/EXT, the LFO, EXTERNAL GATE/CLK IN, or -AGATE will also trigger and gate the envelopes or advance the sequencer.

LFO squarewave output passes through J3 GATE/CLK IN contacts. The CLOCK signal normally toggles inverter U114-4. If an external audio source has been connected to J7 AUDIO IN (discussed above), -EXT is low, grounding pin 5 through D115 and forcing U114 high. This allows the -AGATE signal from the AUDIO GATE CPR (discussed above), to toggle inverter U114-2. Whatever the source, this output sets or resets the microcomputer's internal flag bit through U113-13, T1.

When the Sequencer or Arpeggiator are being used, S125B or S127B hard-synchronizes the LFO to the GATE. When GATE is low, R1101 and R1102 charge C129. When GATE goes high, it pulls Q102 base to ground, switching Q102 on, and discharging the LFO's timing capacitor (in the same manner as OSC A is synced to OSC B).

2-15 POWER SUPPLY

The power supply design is straightforward. As shown on the inset on schematic SD121, the primary circuitry was originally included on the PCB itself (Revisions 1.0 and 1.1). This proved to be mechanically unreliable, most frequently resulting in broken power switches. Section 4 gives the recommend fix for this problem. Current production Pro-Ones, designated Revision 1.2 have all of the power supply primary circuitry moved from the PCB to the back panel.

If any regulators are replaced, a complete functional test will be needed. The slightest change in supply voltage will affect all tuning adjustments and offsets such as the Final VCA Balance.

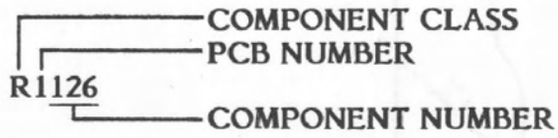
3-0 DOCUMENT LIST

FIG. 3-0	INTERCONNECT DIAGRAM
FIG. 3-1	CONTROL IDENTIFICATION
PP131	PARTS PLACEMENT
SD121	MICROCOMPUTER, KEYBOARD, MODULATION, LFO, POWER
SD112	OSCILLATORS, FILTER, AMPLIFIER, ENVELOPE GENERATOR

3-1 DOCUMENT NOTES

These notes explain component designation and symbol use on our documentation. Abbreviations are decoded in the Glossary.

Component designators include three items of information:



Component Class is symbolized by U.S. industry-standard letters, for example, U for integrated circuit, Q for transistor, and DS for indicator. Component class letters are so identified in the Glossary.

The Pro-One has only one PCB, so the PCB number is one in all cases. No PCB Number is given for chassis-mounted components. (Al though the back-panel jacks mount directly to the PCB, for designation they are considered to be chassis-mounted.)

Component Numbers are sequenced according to their position on the original PCB. When it sometimes becomes necessary to later add a component to the PCB, its designator will usually not be in sequence. This helps identify the modification.

Signals are continued between pages as shown here. Note that the destination or source is always given. The pointers indicate signal flow.

Connectors are drawn according to whether the pins are male or female, so the arrows do not necessarily indicate signal flow. Zeros are slashed only where needed to prevent ambiguity.

Power and ground connections for multi-device ICs are shown on the first device in the package, except where the first device is not presently used.

Unless otherwise indicated, resistances are in ohms and capacitances in microfarads.

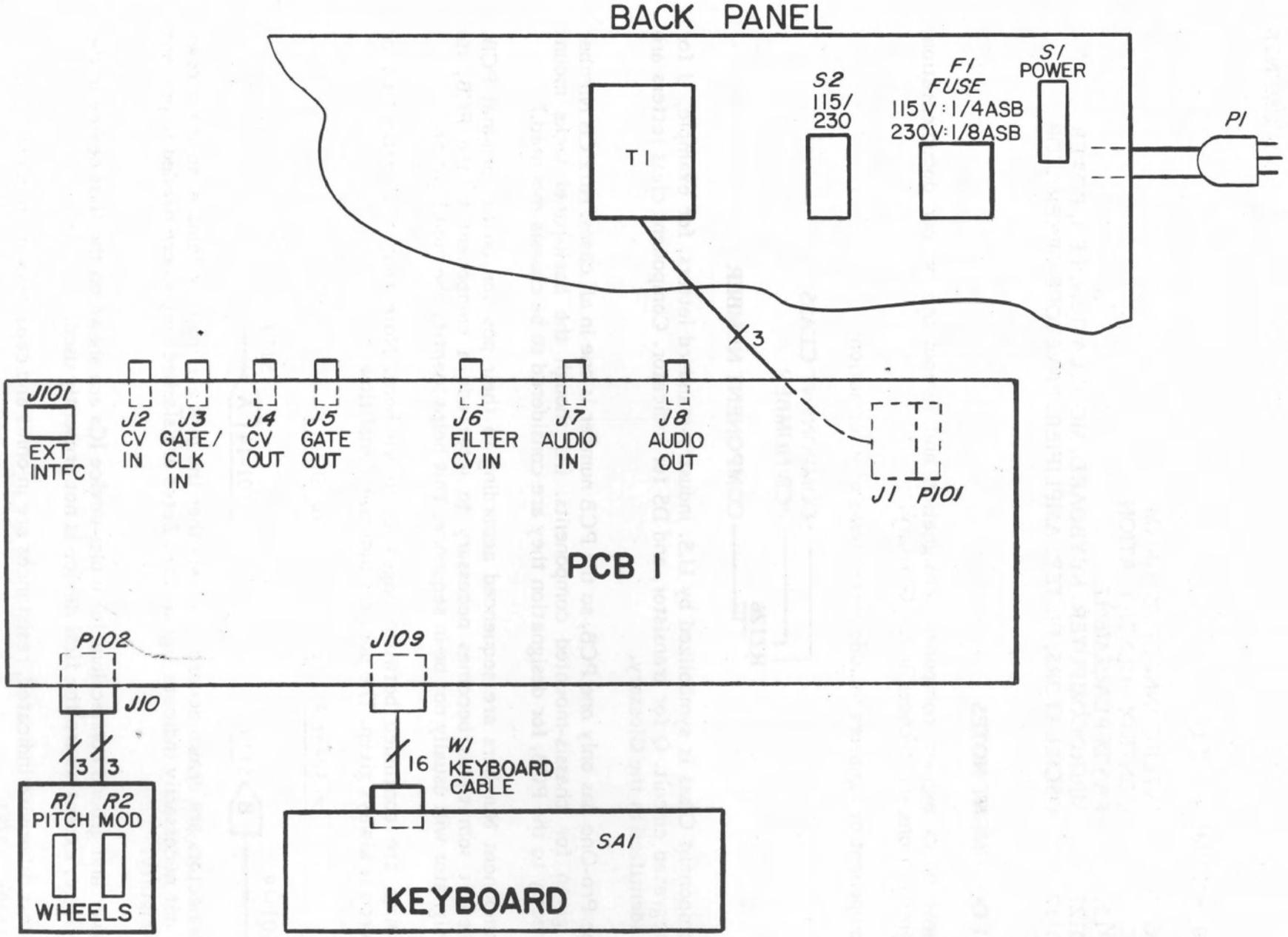


FIGURE 3-0 INTERCONNECTION

MODULATION
FROM
TO
WHEEL
DIRECT
AMOUNT
ROUTE
FIL ENV
OSC B
LFO
OSCILLATOR A
FREQUENCY
OCTAVE
SHAPE
PULSE WIDTH
SYNC
OFF
OSCILLATOR B
LO FREQ
KYBD
NORMAL
MIXER
OSC A
OSC B
NOISE
GLIDE
AUTO
RATE
FILTER
CUTOFF
RESONANCE
ENVELOPE AMOUNT
KEYBOARD AMOUNT
ATTACK
DECAY
SUSTAIN
RELEASE
MASTER TUNE
FO/CLOCK
SEQUENCER
SEQ 1
SEQ 2
RECORD
PLAY
ARPEGGIATE
UP
UP/DOWN
MODE
RETRIG
REPEAT
KEY
GATE
AMPLIFIER
VOLUME

J101
J102
J103
J104
J105
J106
J107
J108
J109
R101
R102
R103
R104
R105
R106
R107
R108
R109
R110
R111
R112
R113
R114
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R1124
R1125
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R1127
R1128
R1129
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R1169
R1170
R1171
R1172
R1173
R1174
R1175
R1176
R1177
R1178
R1179
R1180
R1181
R1182
R1183
R1184
R1185
R1186
R1187
R1188
R1192
R1196
R1197
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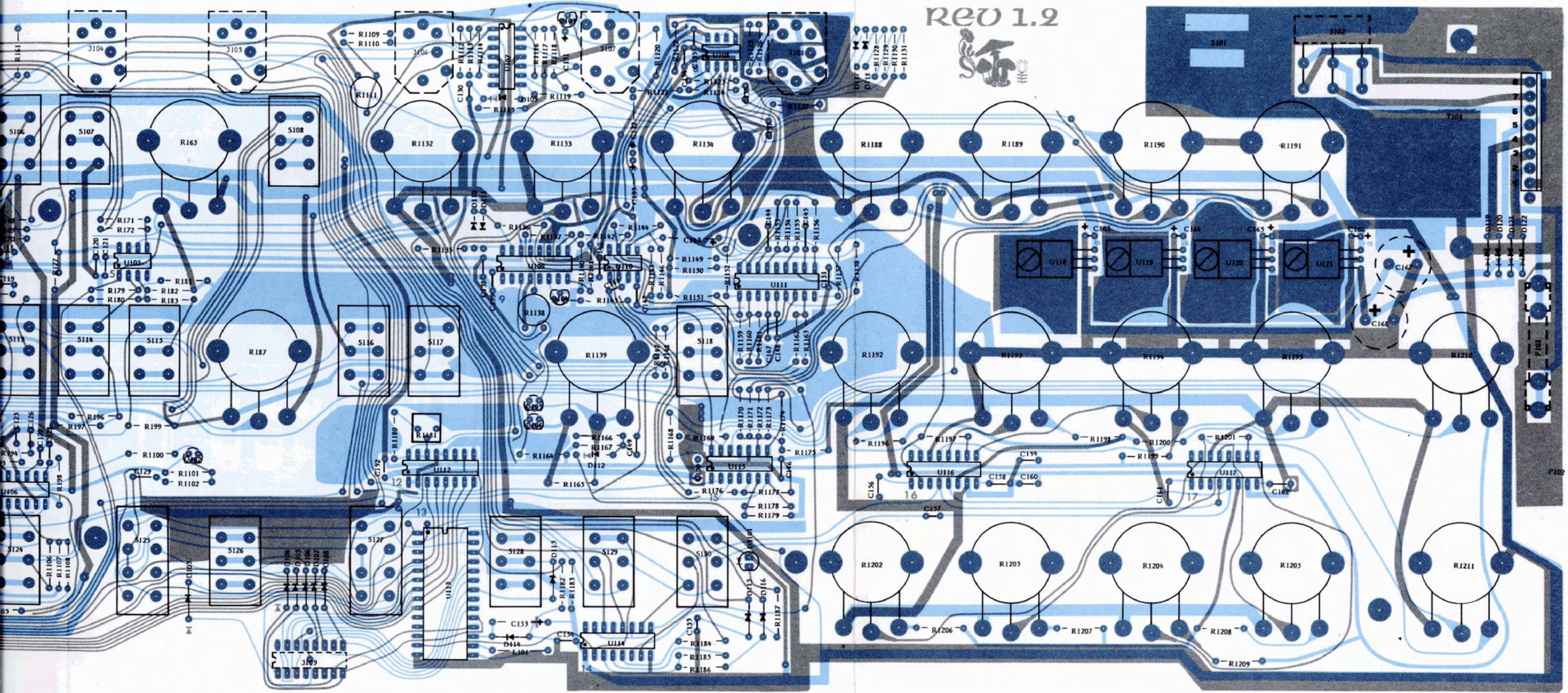
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A

U113 MICROCOMPUTER

8021

+5V

Vcc 28

XTAL 1 15

XTAL 2 16

L101 470 µH

PROG 3

ALE 12

RESET 17

D114 IN914

P00 4
P01 5
P02 6
P03 7
P04 8
P05 9
P06 10
P07 11
P10 18
P11 19
P12 20
P13 21
P14 22
P15 23
P16 24
P17 25
P20 26
P21 27
P22 1
P23 2

DAC EN

GATE

TRIG

T1

Vss 14

J109 W1

KYBD/SWITCH MATRIX SAI-KEYBOARD

C0 C#0 D0 D#0 E0 F0 F#0 G0
G#0 A0 A#0 B0 C1 C#1 D1 D#1
E1 F1 F#1 G1 G#1 A1 A#1 B1
C2 C#2 D2 D#2 E2 F2 F#2 G2
G#2 A2 A#2 B2 C3

16 2 15 1 14 10 9 6 8 7 5 4 3

SI25A SEQ 1 D105
SI25A SEQ 2 D104
SI27A ARP UP D107
SI27A ARP UP/DOWN D109
SI28 MODE RETRIG D113
SI26 RECORD D106

(D103) (IN914) (ARP DOWN)

J101 7

TRIG

⚠ MODE REPEAT/EXT

SI29 REPEAT NORM

CLOCK IN

MODE DRONE SI30 DRONE OFF

TO C157 ENV GENS

GATE B U117-4

⅙ U114 GATE LED DRIVER

DSI01 GATE

R1183 10K

¾ U114 INV

GATE OUT J5

GATE DRIVER

U107-1 B AGATE D116 IN914

FROM J7 B EXT AUDIO IN D115 IN914

R1186 15K
R1185 10K
R1184 24K

⅙ U114

C154 .001

J3 GATE/CLK IN

REPEAT/EXT DRIVER

C155 .001

LFO ⊓

U112 DAC

AD558

DB0 1
DB1 2
DB2 3
DB3 4
DB4 5
DB5 6
DB6 7
DB7 8

C1 9
Vcc 11
+15V C152
CS 10
GND 12
GND 13
V OUT 16
V SENSE 15
V SEL 14

D5 D4 D3 D2 D1 D0
1 2 3 4 5 6
DAC EN 8 J101

14 13 12 11 10 9 J101

(SEE ALSO U113-1)

- GATE

+15V +5V

R1167 390K 4.3V
D112 IN914
C149
S118 AUTO NORMAL GLIDE
+5V
R1166 160K
0-0.3V
R1165 13K
R1139 100K LIN CW
GLIDE RATE

+15V R1164 30K 62V

Q105 2N4250
Q106 2N4250 CURRENT SOURCE

½ U110 GLIDE BUFFER

½ U109 GLIDE OTA

+15V C138 .1

R1135 10K
R1180 1.5K 1%
D110 IN914
D111 IN914
R1181 DAC SCALE 1K
R1136 10K

Id Iabc 3280 V+ V-

NC NC

+15V C140 .1
TL082 -15V C142 .1
C141 .01 mylar

GLIDE CIRCUIT

(1-4V)

R1176 10K 1%
R1177 150K 1%

(0-3V)
R1178 10K 1%
R1179 150K 1%

LM348 ¼ U115 1V SUBT'R

+15V C150 .1
LM348 -15V C151 .1

¼ U115 CV OUT DRIVER

J4 CV OUT
B R121
B J6 BD CV
J2 CV IN

U106 LFO

+15V C123 .1

R193 30K
R192 5.1K
C124 .1
R190 820K
-5V

LFO FREQUENCY R160 100K LIN
R191 200K

+15V R195 470 C125 .01
R189 2.2M
+15V R194 470 C126 .01
R1108 62K
R1107 12K
R1106 820K

(R1182) (10K) ⚠

3340

TCO 1
TCO 2
V- 3
SUM 15
H SYNC 6
LFM 13
S SYNC 9
PW MOD 5
HI FREQ GND 7
EXP CV 14
CF 12
V+ 16

C128 .1
R198 1.8K
C127 .01

LFO Λ S122 R151 100K
LFO ⊓ S124 R152 200K
LFO V S123 R116 100K

R1103 10K
R1105 100K
R1104 560K -15V
R115 33K

¼ U101 LFO SUMMER

R114 100K
LM348

R1100 820
Q102 2N3904
R1102 10K
R1101 47K
-5V

U116-2 B FILT ENV
U105-1 B OSC B

SI25B SEQ 1 OFF
SI27B UP OFF
C129 200pF
SEQ 2 UP/DOWN
SEQ ARP

MOD LFO AMT R103 100K LIN
SI20 WHEEL DIRECT LFO ROUTE R108 100K
R107 100K

MOD FILT ENV AMT R101 100K LIN
SI03 WHEEL DIRECT FILT ENV ROUTE R111 100K
R105 100K

MOD OSC B AMT R102 100K LIN
SI10 WHEEL DIRECT OSC B ROUTE R110 100K
R106 100K

J10 R2 MOD WHEEL 100K LIN

R109 220K +15V C101 .1
¼ U101 W-MOD SOURCE BUFFER
LM348 C102 .1 -15V
R104 43K
P102

¼ U101 W-MOD FOLLOWER
LM348

WH B SI19 (OSC A/B)
WH B SI21 (FILT)

R112 68K
¼ U101 DIRECT SOURCE BUFFER
LM348
R113 68K
DIR B SI19 (OSC A/B)
DIR B SI21 (FILT)

⚠ OPTIONAL FOR DIGITAL INTERFACE

REV. 1.1 POWER SUPPLY PRIMARY

T101 TRANSFORMER

SI02 115 230
U14A, SLO-BLO 230V; 1/8A, SLO-BLO
LINE VOLTAGE
POWER 240
18V 18V
P1 J01 P102

T1 TRANSFORMER

A J1 B P101

S2 115 230
F1 1/4A, SLO-BLO 230V; 1/8A, SLO-BLO
LINE VOLTAGE
POWER S1
AC IN P1

8 5 (KEYED) NC 2 NC
7 18V
6 1
2 18V
5 4

D122 D121 D119 D120 (4 x IN4002)

U121 78M15 +15V
C168 2200 25V
C166 2.2 25V tant

U120 78M05 +5V
C165 2.2 10V tant

U119 7905 -5V
C167 2200 25V
C164 2.2 10V tant

U118 79M15 -15V
C163 2.2 25V tant

LAST	NOT USED
C 168	
D 122	
F 1	
J 109	
P 102	
Q 106	
R 1211	R1000-1009
S2	
SA 1	
U 121	
DSI01	
L 101	
T1	
W1	
J3	

123 (FRONT)

REVISION	DATE	BY
8-5-81	06	J1 WAS NOT KEYED
5-13-81	94A	MOVED TO CHASSIS

SEQUENTIAL CIRCUITS INC

TITLE: MICROCOMPUTER, KEYBOARD, LFO, MODULATION, POWER SUPPLY

DSN
DWG
APP
ISS

SIZE D MODEL No. 100 1.2
DATE 12/1/80
DOCUMENT No. SD 121
SHEET 1 OF 1

OSC A OCTAVE
OSC A FREQUENCY
OSC A OFFSET
MASTER TUNE
OSC A OCTAVE
PITCH WHEEL
KYBD CV
FROM J2 CV IN
OCTAVE SUMMER
MOD TO OSC A FREQ
MOD TO OSC A PW
OSC A PULSE WIDTH
OSC A PW SUMMER
OSC A SCALE
HI TRIM
OSC A SYNC
OSC A Λ
OSC A ⊓
OSC A SUMMER
MIX OSC A
PITCH WHEEL
DEADBAND
MASTER TUNE
OSC B OCTAVE
OSC B FREQUENCY
LO FREQ
NORMAL
OSC B OCTAVE SUMMER
OSC B KEYBOARD
MOD TO OSC B FREQ
MOD TO OSC B PW
OSC B OFFSET
OSC B PULSE WIDTH
OSC B PW SUMMER
OSC B SCALE
OSC B Λ
OSC B ⊓
OSC B
OSC B SUMMER
MIX NOISE/EXT
-1V BUFFER
-1 VOLT TRIM
AUDIO IN (MONO ONLY)
NSE PREAMP
NOISE/EXT PREAMP
MIX OSC B
AMP ATTACK
AMP DECAY
AMP SUSTAIN
AMP RELEASE
AMP ENV GEN
TRIG
GATE
DRONE SWITCH
RESONANCE
4-POLE LOW-PASS FILTER
FILT BFR
FIN VCA
AUDIO DRIVER
VCA BAL
AUDIO OUT
ENVELOPE FOLLOWER
AUDIO GATE CPR
FILTER SMR
CUTOFF
MOD TO FILTER
FILTER CV IN
KEYBOARD AMOUNT
VOLUME
FILTER ATTACK
FILTER DECAY
FILTER SUSTAIN
FILTER RELEASE
FILT ENV GEN
ENVELOPE AMOUNT
TRIGGER
GATE
-EXT
-AGATE
4 x 150 PF disk
A/B MATCHED TO .01%

SEQUENTIAL CIRCUITS INC

TITLE: OSC, FILTER, AMP, ENV GEN

8-4-81	103	R1120 WAS 100K	
4-8-81	79	R1212 WAS 1M	
3-10-81	79	R124/R144 WERE 1.5M	
3-18-8	73	R1196/R1205 WERE 2M	
DATE	ECR No.	REVISION	LTR

DSN
DWG Jay Chambers 11/5/81
APP
ISS

SIZE D | MODEL No. 100 | DOCUMENT No. SD112 | SHEET 1 OF 1

SECTION 4

MECHANICAL

4-0 INTRODUCTION

The Pro-One has been produced in two basic versions. Revisions 1.0 (prototype) and 1.1 (production) include the entire power supply on the PCB. Besides the increased shock hazard, shipping realities revealed two weaknesses in this design. Held by only its terminals, the transformer (SCI #E-011) tended to break off. Also, the power switch (#S-048) was often being damaged. Therefore in revision 1.2, the power supply primary circuitry was moved to the back panel. There have been no problems with the new design.

It is easy to distinguish between the two versions. Revision 1.2, requiring no modifications, can be identified by the presence of the fuseholder on the back panel.

Depending on whether or not it has been previously serviced, a revision 1.0/1.1 unit may or may not need further modification. SCI Authorized Service Centers have been instructed to bolt the transformer to the PCB with 4-40 metal hardware (you may find nylon hardware on some units). The metal screw head and nut must be insulated from the transformer and PCB with fiber washers. Also, to reduce the possibility of switch breakage, we have recommended enlarging the hole for the power switch, and glueing the top of the switch.

While these modifications have provided adequate protection for most units, a more secure mounting for revision 1.0/1.1 PCBs is described in para. 4-2. Inspection and modification of the primary power connector system is also covered.

4-1 OPENING CASE AND REMOVING PCB

1. Switch power off.

2. Unplug power cord and disconnect all cables to the back panel.

3. Remove wooden side panels (2 screws each side).

4. Remove three screws along front edge. (If the unit has been modified as described in para. 4-2, then also remove 8-32 screw near power switch.)

5. Carefully slide top panel assembly forward. When front edge is clear of keys, lift it up just enough to allow clearance for your hand.

6. Reach in and disconnect AC power connector running from back panel to underside of printed circuit board (PCB), at right. (When reconnecting, orient connector so the side through which you can see the metal contacts is visible.)

7. Also disconnect keyboard cable from PCB. (When reconnecting, the keyboard cable should be twisted so that the ribbon crosses over the board. If correct, the numbers 9-16 stamped on the connector will run along the PCB edge.) The top panel assembly will now lift away.

8. Pull off all knobs.

9. Disconnect wheel connector at left of PCB. (When reconnecting, orient connector so that the side in which you can see the metal contacts is visible.)

10. Remove 9 screws holding PCB to top panel (there are two screws near the transformer).

11. The PCB should now lift away from the top panel. If not, check that the GATE LED is not stuck or cemented.

12. Set the PCB on insulation on the bottom panel, and reconnect AC and keyboard. Switch power on and, if tuning, allow the instrument to warm up for at least fifteen minutes before proceeding.

WARNING! LETHAL VOLTAGE IS PRESENT IN THE POWER SUPPLY AREA ON THE PCB (IN EARLIER MODELS) OR ON THE BACK PANEL (IN LATER MODELS).

4-2 REVISION 1.0/1.1 PCB MOUNTING MODIFICATION

To adequately protect the power switch on early Pro-Ones, an additional bracket must be retro-fitted to eliminate vertical movement resulting from PCB flexibility. Figure 4-1 shows four views of the modification. Order Bracket Kit SCI #Z-204.

1. Open the Pro-One and remove PCB as described in para. 4-1.

2. Drill two holes through PCB as shown in Figure 4-1A.

3. Attach bracket M-323 to PCB underside using two M-100 #4-40 x 3/8" (9,525 mm) screws, two M-141 starwashers, and two M-099 4-40 nuts as shown in Figure 4-1B.

4. Install PCB into top panel, tightening the 9 screws.

5. Drill hole through back panel as shown in Figure 4-1C. (Be sure to remove all loose metal.)

6. When fastening the top and bottom assemblies, first install M-089 #8-32 x 3/8" (9,525 mm) screw as shown in Figure 4-1D. Then install the remaining seven chassis screws.

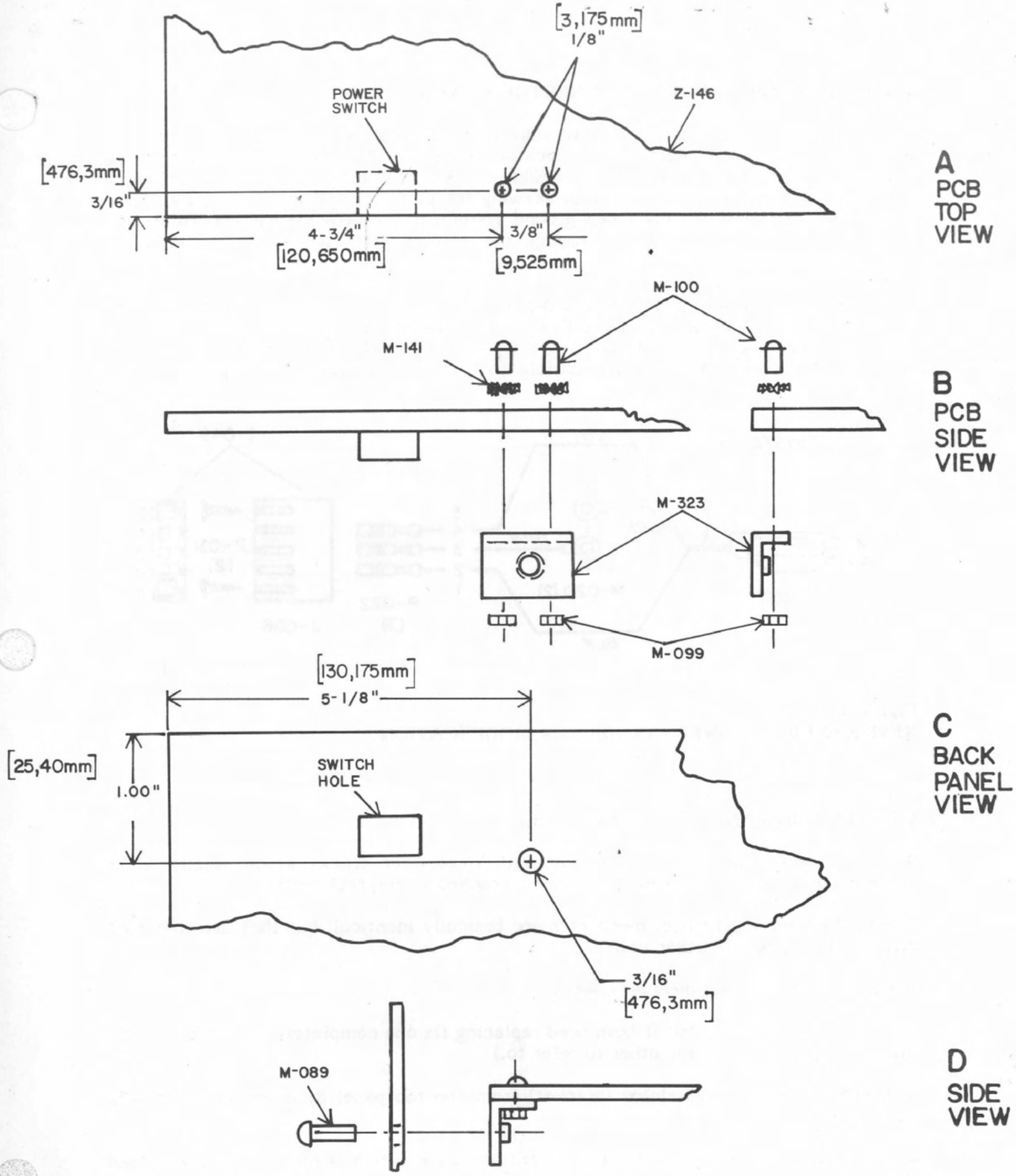


Figure 4-1
REVISION 1.0/1.1 PCB MOUNTING MODIFICATION

4-3 REVISION 1.0/1.1 POWER CONNECTOR MODIFICATION

It also turns out that the original version of the Pro-One's power connector (to the PCB) is not foolproof. Particularly because you can't see what you are doing when you're reassembling a unit, it is possible to incorrectly mate the female cable connector to the male PCB header by skewing the pins. This can result in applying one side of the ac line to the Pro-One's ground system. If the Pro-One happens to also be grounded to external equipment through the AUDIO OUT connection, the resulting high currents will destroy the PCB.

The problem is corrected by using a 5-pin female connector keyed at both ends, as shown in Figure 4-2. If a 1.0/1.1 Pro-One being serviced has either a 3- or 4-pin female connector, remove them and install the 5-pin connector system (order SCI #Z-049). With the 5-pin system it is still possible to reverse the connection, but this won't damage anything.

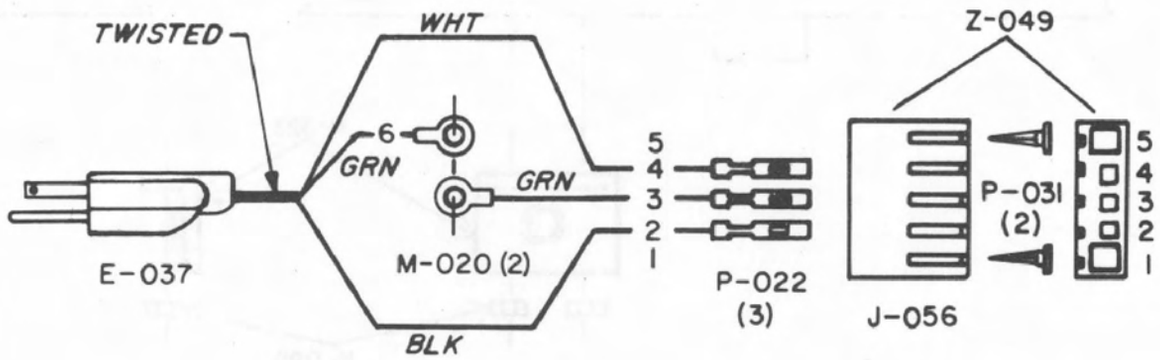


Figure 4-2
REVISION 1.0/1.1 POWER CONNECTOR MODIFICATION

4-4 REPLACING AND ADJUSTING WHEELS

Whenever you open the case, inspect both wheels for cracks which usually occur perpendicular to the set screw. If you see a cracked wheel, replace it.

The PITCH and MOD wheel mechanics are basically identical, but they are trimmed differently. To repair either wheel:

1. Open the Pro-One as directed above.

2. Inspect both wheels, but if both need replacing fix one completely first, then fix the other. (So you can have the other to refer to.)

3. Remove the wheel assembly (bracket) from the top panel by unscrewing the 6-32 hardware.

4. Look at the wheel assembly. The potentiometer rotation is limited by two molded stops on the wheel. When replacing with a new wheel (SCI #M-352), be sure the limiting stops are correctly oriented.

5. Use the set screw from the old wheel if necessary. But don't fully tighten it yet--the wheel still must be trimmed.

6. Reinstall the wheel assembly (bracket) into the top panel. Make sure everything is safe and switch power on. Trim according to steps 7 or 8 as required.

7. R1 PITCH wheel is supposed to contribute 0 volts when centered. So probe P102-6 (or the wiper of R1 itself) with DVM. With one hand, hold the wheel firmly in center-detent position. Use a screwdriver to trim the shaft of R1 to read as close as possible to 0V. Move wheel up and down, trimming for best repeatability of 0V at center-detent, then tighten set screw. (The "deadband" diodes following R1 make this trim much less critical.)

8. R2 MOD wheel must be able to turn off fully. To trim, simply make sure the wiper is fully grounded when the wheel is fully down.

5-0 INTRODUCTION

This section contains full tuning and trimming procedure as well as instructions for using the Digital Interface.

5-1 DAC SCALE

This adjustment should not be performed as part of the tuning procedure. In fact, readjustment may only be necessary if a repair has been made. Whenever this adjustment is made the Pro-One will have to be completely retuned. A 3-1/2 digit voltmeter (DVM) is required.

1. Connect DVM to back-panel CV OUT jack.

2. Hit C0 and note reading. The reading will be approximately 0.083V. (The absolute value of this reading is not critical.)

3. Hit C3 and note reading, which should be the value read in step 2, plus exactly 3V. If necessary, adjust R1181 DAC SCALE for the exact reading; e.g. 3.083V.

4. Repeat steps 2 and 3 as required to establish an exact 3-V difference between CV OUT played by C0 and C3.

5-2 TUNING

1. Patch according to Figure 5-0. Start a full tuning by presetting both R120 OSC A and R140 OSC B OFFSET trimmers to the middle of their range. For component locations, see Figure 5-1.

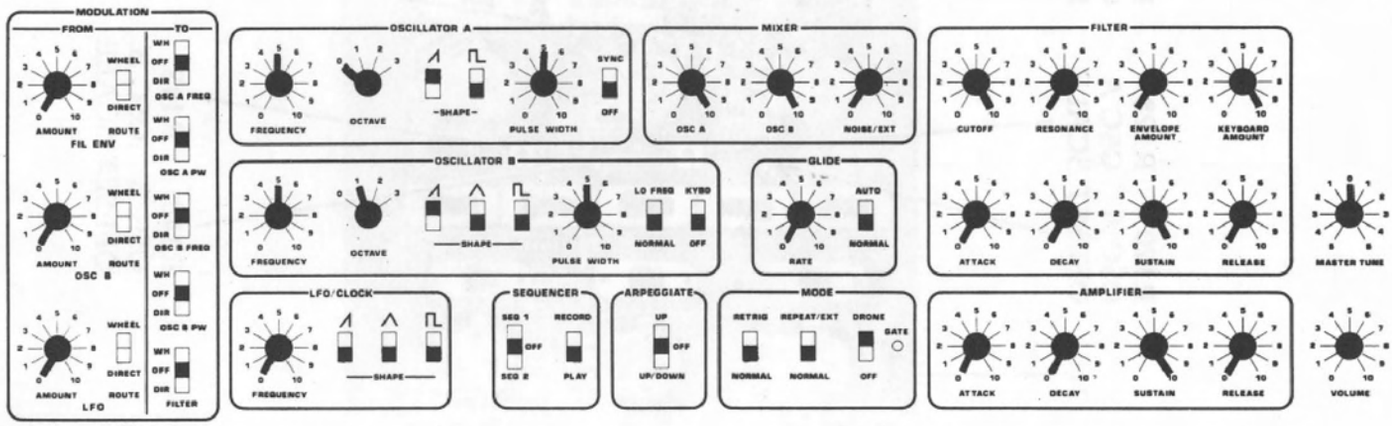
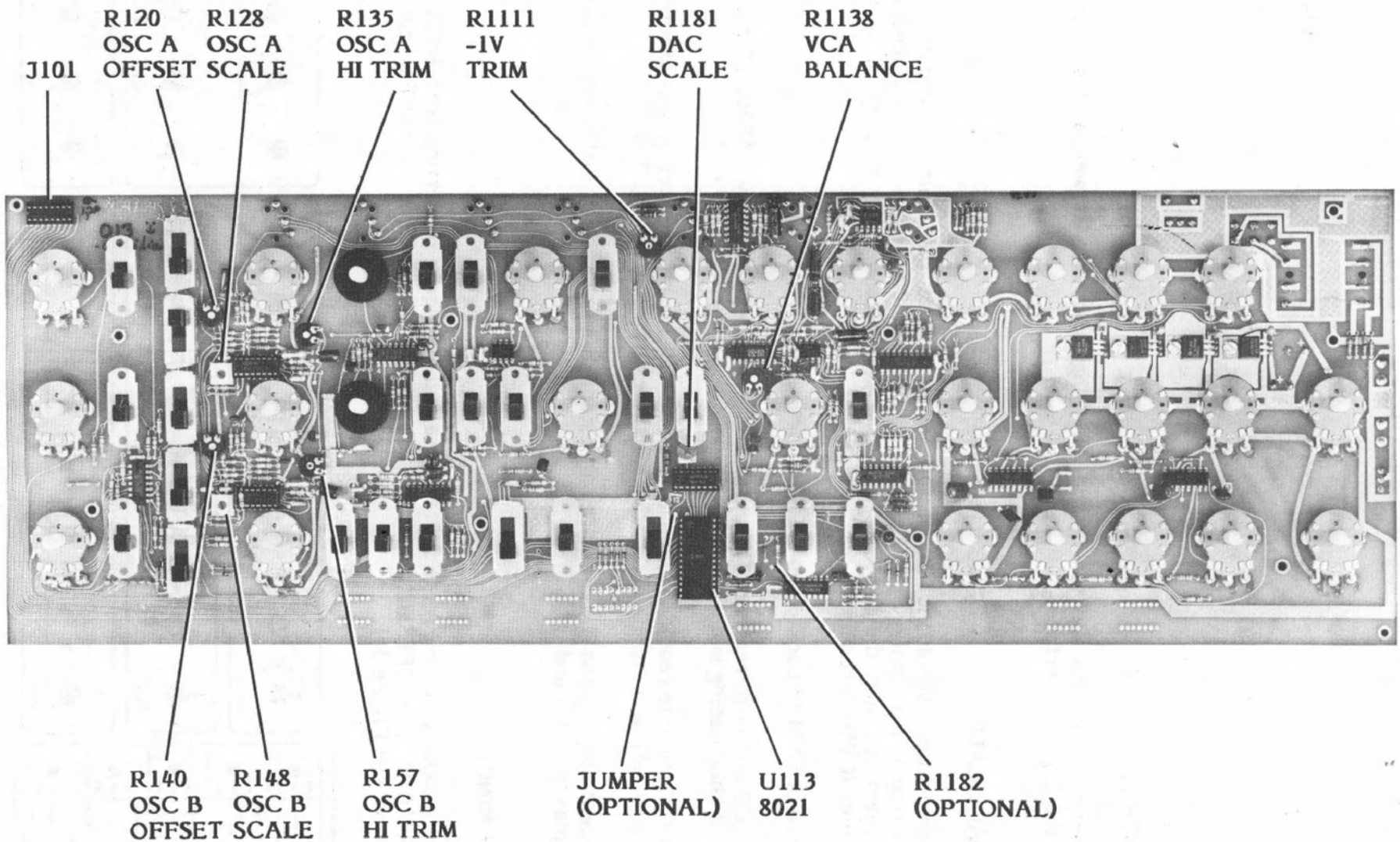


Figure 5-0
TUNING PATCH

Figure 5-1
PCB



--OSC A SCALE--

2. Hit C0 and adjust OSC A FREQUENCY for zero-beat.

3. Hit C3 and adjust R128 OSC A SCALE for less than 1 Hz beating.

4. Repeat steps 2 and 3 until no further improvement can be made.

--OSC A HI TRIM--

5. Switch OSC A OCTAVE to 3.

6. Switch OSC B OCTAVE to 3.

7. Hit C0 and adjust OSC A FREQUENCY for zero-beat.

8. Hit C3. Adjust R135 OSC A HI TRIM for zero-beat.

9. Repeat steps 7 and 8 until no further improvement can be made.

-- -1V TRIM--

10. Switch OSC A OCTAVE to 0.

11. Switch OSC B OCTAVE to 1.

12. Hit C0 and adjust OSC A FREQUENCY for zero-beat.

13. Switch OSC A OCTAVE to 3 and adjust R1111 -1V TRIM for zero-beat.

14. Switch OSC A OCTAVE to 1 and 2 and check for less than 2 Hz beating.

--OSC B SCALE--

15. Switch OSC A OCTAVE to 1.

16. Switch OSC B OCTAVE to 1.

17. Turn OSC A FREQUENCY to 5.

18. Turn OSC B FREQUENCY to 5.

19. Switch OSC B KYBD on.

20. Hit C0 and adjust OSC B FREQUENCY for zero-beat.

21. Hit C3 and adjust R148 OSC B SCALE trimmer for less than 1 Hz beating.

22. Repeat steps 20 and 21 until no futher improvement can be made.

--OSC B HI TRIM--

23. Switch OSC A OCTAVE to 3.

24. Switch OSC B OCTAVE to 3.

25. Hit C0 and adjust OSC B FREQUENCY for zero-beat.

26. Hit C3 and adjust R157 OSC B HI TRIM for zero-beats.

27. Repeat steps 25 and 26 until no further improvement can be made.

--OSC A/B OFFSET--

28. Check that PITCH WHEEL and MASTER TUNE are centered.

29. Switch OSC A OCTAVE to 1.

30. Turn OSC A FREQUENCY to 0.

31. Switch OSC B sawtooth off.

32. Using an external reference (tuning fork, piano, or Prophet), adjust R120 OSC A OFFSET so key A2 pitch is A-440.

33. Switch OSC A OCTAVE to 3.

34. Switch OSC B OCTAVE to 3.

35. Turn OSC B FREQUENCY to 0.

36. Switch on OSC B sawtooth.

37. Hit C1 and adjust R140 OSC B OFFSET for zero beats.

5-3 AMPLIFIER BALANCE

1. Patch according to Figure 5-2.

2. Increase system volume to fairly high level. Adjust R1138 VCA BALANCE for minimum envelope bleed-through.

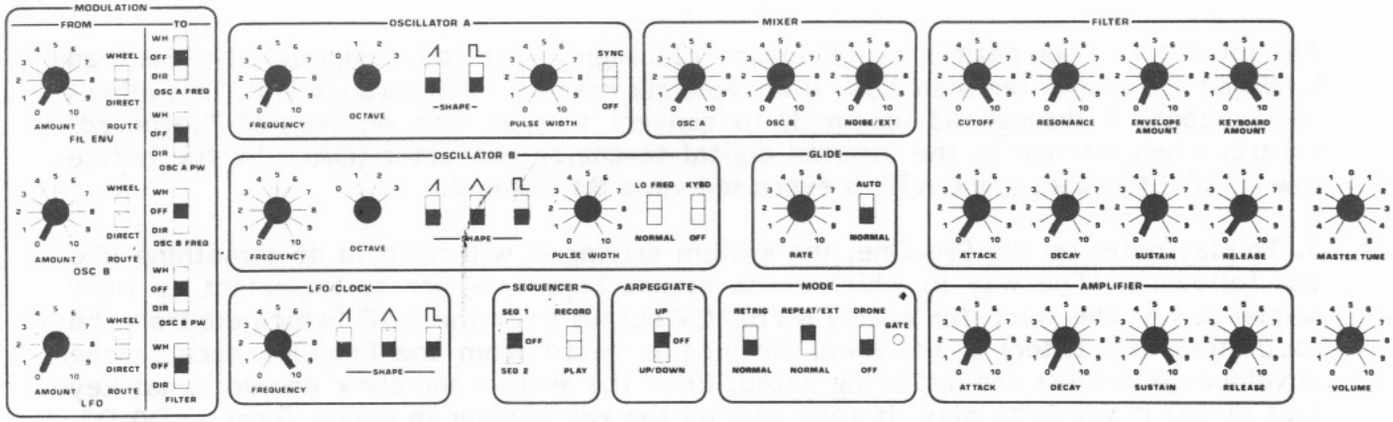


Figure 5-2
AMPLIFIER BALANCE PATCH

5-4 DIGITAL INTERFACE

Use of the digital interface for external computer control requires both some simple hardware modifications to the Pro-One and the creation of software for your system. If you doubt your technical ability to install the interface, please see an SCI Authorized Service Center or contact our Service Department. However please note that we must leave all questions of programming your system to you.

1. Remove U113 (see Figure 5-1) 8021 microcomputer from its socket. Keep it safe. Note that with the 8021 removed, the Pro-One's keyboard cannot operate.

2. Jumper pin 2 of the 8021's socket to J101-7. Pads are provided on the printed circuit board (PCB) for this purpose.

3. Add R1182, 10K-ohm, 1/4W, 5% resistor where shown on Figure 5-1.

4. Table 5-0 lists pin assignments. Mate J101 with a 14-wire ribbon cable terminated in a DIP plug. (There are six spare lines.)

Table 5-0
J101 DIGITAL INTERFACE PINS (J101)

1	D5
2	D4
3	D3
4	D2
5	D1
6	D0
7	GATE
8	-DAC EN
9-14	GROUND

The interface is compatible with standard TTL logic, where a 0 is signified by less than 0.8V and a 1 by greater than 2.5V. It accepts six data bits (D0 through D5). This allows the numbers 0 through 63 (decimal) to convert to over five octaves of "keyboard" control when latched to the internal digital-to-analog converter (DAC) by the active low -DAC EN pulse. The GATE is exercised via a bit at pin 7.

5. To play notes on the Pro-One, the system driving it will have to do something like the following. (The way in which these events happen is not so important as their sequence.) At the start, the analog KYBD CV output from the DAC (which controls the oscillators and filter) is unknown. Nothing is heard from the Pro-One because the envelope generators are not being gated. First the system somehow decides what key (out of 63) it wants to play. It then sets up the key number in binary form on D0-D5. (This might be done with a six-bit output port.) -DAC EN is normally high. To latch the key data to the DAC, -DAC EN is momentarily forced low. Data is then latched on the rising edge of this pulse. For practical purposes a delay of 20 microseconds will allow the DAC time to "settle" (worst-case). At this point, GATE can go high, triggering the envelope generators. When the note is to be turned off, it is likewise advisable to turn the GATE off (low) before again strobing the DAC.

6. To return the Pro-One to normal operation, unplug your system from J101, remove R1182, cut the jumper installed in step 3 and carefully re-install U113, 8021.

6-0 CHASSIS

F1 (115V)	E-021 1/4A 3AG
F1 (230V)	E-093 1/8A 3AG
J1	J-056 5-PIN MOLEX HOUSING
J2-6	J-048 MONO PHONE JACK, PCB, SHORTING
J7/8	J-049 STEREO PHONE JACK, PCB, SHORTING
J10	J-030 6-PIN MOLEX HOUSING
P1	E-037 POWER CORD
R1/2	R-207 100K WHEEL POT
S1	S-054 POWER SWITCH
S2	S-032 115/230 SWITCH
SA1	S-050 KEYBOARD
T1	E-102 36 VCT TRANSFORMER
W1	E-075 11" 16-WIRE DIP RIBBON

CHASSIS HARDWARE

E-017 FUSEHOLDER
E-018 FUSEHOLDER CAP
M-070 #6 SET SCREW
M-073 PITCH WHEEL DETENT CLIP
M-204 BRACKET, WHEEL
M-352 WHEEL, MOLDED
M-357 KNOB

6-1 PCB 1

C101/02	C-045 .1 50V
C103	C-012 .01 50V MYLAR
C104	C-045 .1 50V
C105	C-039 1000 pF POLY
C106	C-012 .01 50V MYLAR
C107/08	C-045 .1 50V
C109/10	C-012 .01 50V MYLAR
C111/12	C-045 .1 50V
C113	C-039 1000 pF POLY
C114	C-012 .01 50V MYLAR
C115	C-045 .1 50V
C116-19	C-008 .001 50V MYLAR
C120	C-045 .1 50V

C121	C-045 .1 50V
C122	C-005 200 pF 50V DISC
C123/24	C-045 .1 50V
C125	C-012 .01 50V MYLAR
C126/27	C-012 .01 50V MYLAR
C128	C-045 .1 50V
C129	C-005 200 pF 50V DISC
C130	C-012 .01 50V MYLAR
C131-33	C-052 2.2 15V ELECT
C134/35	C-045 .1 50V
C136	C-002 10 pF 50V DISC
C137	C-012 .01 50V MYLAR
C138-40	C-045 .1 50V
C141	C-012 .01 50V MYLAR
C142	C-045 .1 50V
C143	C-052 2.2 15V ELECT
C144/45	C-049 150 pF DISC
C146	C-045 .1 50V
C147/48	C-049 150 pF DISC
C149-52	C-045 .1 50V
C153	C-050 1 10V ELECT
C154	C-045 .1 50V
C155	C-008 .001 50V MYLAR
C156	C-043 .039 50V MYLAR
C157	C-012 .01 50V MYLAR
C158	C-014 .02 50V MYLAR
C159/60	C-045 .1 50V
C161	C-043 .039 50V MYLAR
C162	C-014 .02 50V MYLAR
C163	C-021 2.2 25V TANT
C164/65	C-051 2.2 10V TANT
C166	C-021 2.2 25V TANT
C167/68	C-025 2200 25V ELECT
D101-18	D-005 1N914
D119-22	D-001 1N4002 100V 1 AMP
DS101	L-001 LED, LARGE
J101/09	J-007 16-PIN DIP SOCKET
L101	E-094 470 uH INDUCTOR
P101	P-051 4-PIN MOLEX HEADER
P102	P-026 6-PIN MOLEX RIGHT-ANGLE HEADER
Q101	T-003 2N4250
Q102	T-002 2N3904
Q103-06	T-003 2N4250

NOTE: **SCI #R-001 THROUGH R-092 ARE 5%**
R-101 THROUGH R-177 ARE 1%
R-200 THROUGH R-228 ARE POTENTIOMETERS

R101-03	R-228 100K
R104	R-086 43K
R105-08	R-025 100K
R109	R-087 220K
R110/11	R-025 100K
R112/13	R-021 68K
R114	R-025 100K
R115	R-054 33K
R116	R-025 100K
R117/18	R-023 82K
R119	R-228 100K POT LIN NO BUSHING
R120	R-217 100K TRIM 1 TURN TOP-ADJ
R121	R-110 100K
R122	R-006 470
R123	R-044 270K
R124	R-029 1M
R125	R-025 100K
R126	R-061 4.7M
R127	R-110 100K
R128	R-211 5K TRIM 1 TURN TOP-ADJ
R129	R-146 26.7K
R130	R-142 5.62K
R131	R-090 1.2M
R132	R-082 820K
R133	R-110 100K
R134	R-139 1.82K
R135	R-225 25K TRIM 1 TURN TOP-ADJ
R136	R-006 470
R137	R-116 2.21M
R138	R-018 47K
R139	R-228 100K POT LIN NO BUSHING
R140	R-217 100K TRIM 1 TURN TOP-ADJ
R141	R-018 47K
R142	R-110 100K
R143	R-006 470
R144	R-029 1M
R145	R-110 100K
R146	R-061 4.7M
R147	R-025 100K
R148	R-211 5K TRIM 1 TURN TOP-ADJ
R149	R-146 26.7K
R150	R-142 5.62K
R151	R-025 100K
R152	R-026 200K
R153	R-066 300K
R154	R-082 820K
R155	R-110 100K
R156	R-139 1.82K
R157	R-225 25K TRIM 1 TURN TOP-ADJ
R158	R-006 470

R159	R-116 2.21M
R160	R-228 100K POT LIN NO BUSHING
R161	R-025 100K
R162-64	R-110 100K
R165	R-228 100K POT LIN NO BUSHING
R166	R-025 100K
R167	R-110 100K
R168	R-012 10K
R169	R-025 100K
R170	R-092 110K
R171	R-026 200K
R172	R-057 120K
R173-76	R-110 100K
R177	R-015 20K
R178	R-092 110K
R179-81	R-025 100K
R182	R-054 33K
R183	R-026 200K
R184-86	R-025 100K
R187	R-228 100K POT LIN NO BUSHING
R188	R-012 10K
R189	R-030 2.2M
R190	R-082 820K
R191	R-026 200K
R192	R-064 5.1K
R193	R-016 30K
R194/95	R-006 470
R196	R-025 100K
R197	R-084 560K
R198	R-075 1.8K
R199	R-012 10K
R1100	R-083 820
R1101	R-018 47K
R1102/03	R-012 10K
R1104	R-084 560K
R1105	R-025 100K
R1106	R-082 820K
R1107	R-072 12K
R1108	R-020 62K
R1109	R-173 7.50K
R1110	R-126 90.9K
R1111	R-225 25K TRIM 1 TURN TOP-ADJ
R1112	R-025 100K
R1113	R-057 120K
R1114	R-062 5.6K
R1115	R-085 3.9M
R1116	R-026 200K
R1117	R-025 100K
R1118	R-021 68K
R1119/20	R-025 100K
R1121	R-011 4.7K
R1122	R-012 10K
R1123	R-029 1M
R1124	R-035 2.7K

R1125/26	R-008 1K
R1127	R-029 1M
R1128	R-076 27K
R1129-31	R-018 47K
R1132-34	R-228 100K POT LIN NO BUSHING
R1135/36	R-012 10K
R1137	R-026 200K
R1138	R-217 100K TRIM 1 TURN TOP-ADJ
R1139	R-228 100K POT LIN NO BUSHING
R1140	R-015 20K
R1141	R-021 68K
R1142	R-015 20K
R1143	R-067 3.9K
R1144	R-058 240K
R1145	R-021 68K
R1146	R-025 100K
R1147	R-041 150K
R1148	R-057 120K
R1149-51	R-058 240K
R1152	R-087 220K
R1153	R-024 91K
R1154	R-025 100K
R1155	R-009 1.5K
R1156	R-025 100K
R1157	R-026 200K
R1158	R-024 91K
R1159/60	R-025 100K
R1161	R-024 91K
R1162	R-056 51K
R1163	R-031 3K
R1164	R-016 30K
R1165	R-013 13K
R1166	R-065 160K
R1167	R-027 390K
R1168	R-018 47K
R1169	R-008 1K
R1170	R-017 39K
R1171	R-025 100K
R1172	R-018 47K
R1173	R-022 75K
R1174	R-010 2K
R1175	R-026 200K
R1176	R-108 10K
R1177	R-150 150K
R1178	R-108 10K
R1179	R-150 150K
R1180	R-172 1.50K
R1181	R-209 1K TRIM 1 TURN TOP-ADJ
R1182/83	R-012 10K
R1184	R-073 24K
R1185	R-012 10K
R1186	R-014 15K
R1187	R-004 330
R1188-95	R-228 100K POT LIN NO BUSHING

R1196	R-086 43K
R1197	R-073 24K
R1198	R-080 2.0M
R1199	R-026 200K
R1200	R-089 1.8M
R1201	R-073 24K
R1202-05	R-228 100K POT LIN NO BUSHING
R1206	R-089 1.8M
R1207	R-080 2.0M
R1208	R-089 1.8M
R1209	R-026 200K
R1210/11	R-228 100K POT LIN NO BUSHING
R1212	R-082 820K
S101	S-048 SWITCH POWER
(REVISIONS 1.0/1.1 ONLY)	
S103	S-046 SWITCH DPDT SLIDE
S104	S-047 SWITCH DP3T SLIDE
S105	S-052 SWITCH DP4T ROTARY
S106-08	S-046 SWITCH DPDT SLIDE
S109	S-047 SWITCH DP3T SLIDE
S110	S-046 SWITCH DPDT SLIDE
S111	S-047 SWITCH DP3T SLIDE
S112	S-052 SWITCH DP4T ROTARY
S113-18	S-046 SWITCH DPDT SLIDE
S119	S-047 SWITCH DP3T SLIDE
S120	S-046 SWITCH DPDT SLIDE
S121	S-047 SWITCH DP3T SLIDE
S122-24	S-046 SWITCH DPDT SLIDE
S125	S-047 SWITCH DP3T SLIDE
S126	S-046 SWITCH DPDT SLIDE
S127	S-047 SWITCH DP3T SLIDE
S128-30	S-046 SWITCH DPDT SLIDE
T101	E-011 36 VCT TRANSFORMER
(REVISIONS 1.0/1.1 ONLY)	
U101	I-313 LM348 QUAD-741 OP AMP
U102/03	I-321 CEM 3340 VCO
U104	I-313 LM348 QUAD-741 OP AMP
U105	I-312 TL082 DUAL BIFET OP AMP
U106	I-321 CEM 3340 VCO
U107	I-313 LM348 QUAD-741 OP AMP
U108	I-324 NE5532 DUAL LOW-NOISE OP AMP
U109	I-322 CA 3280 DUAL OTA
U110	I-312 TL082 DUAL BIFET OP AMP
U111	I-320 CEM 3320 VCF
U112	I-504 AD558 8-BIT DAC
U113	I-039 8021 PRO-ONE MICROCOMPUTER
U114	I-209 4049 HEX INVERTER
U115	I-313 LM348 QUAD-741 OP AMP
U116/17	I-319 CEM 3310 ENV GEN
U118	I-408 79M15 -15V REG

U119	I-411 7905 -5V REG
U120	I-404 78M05 +5V REG
U121	I-406 78M15 +15V REG

PCB HARDWARE AND SOCKETS

M-031 6-32 LOCKWASHER, EXTERNAL TOOTH
M-035 6-32 NUT, SMALL
M-071 6-32 X 1/4" PHS
J-007, 16-PIN DIP
J-045, 28-PIN DIP (FOR U113)

SECTION 7

GLOSSARY

This list covers abbreviations appearing on SCI documentation except that ICs are generally shown with their manufacturers' symbology. Refer to the device data sheet as required.

A	address bus
A	VCO A
A	Ampere
(a),(A)	analog (for power or common)
ac	alternating current
ACC	accumulator
ACK	acknowledge
A/D	analog/digital (hybrid)
ADC	analog-to-digital converter
ADJ	adjust
ADPT	adapter
ADSR	attack/decay/sustain/release (ENV GEN)
AH	address bus, high-voltage
ALU	arithmetic-logic unit
AM	ammeter
AMP	amplifier (FIN VCA)
AMT	amount
APPROX	approximate
ASSY	assembly
ATK	attack
ATT	attenuation, attenuator
AUX	auxiliary
AVG	average
B	VCO B
B	bit number (LSB, MSB)
BAL	balance
BCD	binary-coded-decimal
BFR	buffer
BLK	black
BLU	blue
BRN	brown
BT	battery (designator)
C	capacitor (designator)
C	control (solid-state switch)
C	Centigrade
CAL	calibration, calibrator
CASS	cassette
CB	circuit breaker (designator)
CC	control current for OTAs
CCW	counter-clockwise
CHG	charge

CKT	circuit
CLK	clock
CLR	clear
cm	centimeter
CM	current mirror
CMOS	complementary MOS
CMP	compensation
CNT	count
CNTR	counter
COAX	coaxial
COMM	common
COMP	computer
CONT	control
CONV	conversion, converter
CPR	comparator
CPU	central processor unit
CR	rectifier module (designator)
CS	chip select
CTF	cutoff
CTR	center
CV	control voltage
CW	clockwise
CY	carry
D	data
D	diode (designator)
(d), (D)	digital (power or ground)
DA	diode array (designator)
DAC	digital-to-analog converter
dB	decibel
DB,DBUS	data bus
DBH	data bus, high-voltage
dc	direct current
DCOD	decoding, decoder
DET	detection, detector
DI	data in
DIP	dual in-line plastic (package)
DIS	disable
DISCHG	discharge
DMUX	demultiplexing, demultiplexer
DO	data out
DN	data, non-volatile
DRAM	dynamic RAM
DRVR	driver
DS	indicator (designator)
DSP	display
DVM	digital voltmeter
DX	switch matrix row
DY	switch matrix column
EDIT	edit
EN	enable
ENV	envelope
EOC	end-of-conversion

EOT	end-of-tape
EPROM	erasable-programmable ROM
EQ	equalization, equalizer
EXT	external
F	Farad
F	fuse (designator)
*F	Farenheit
FDBK	feedback
FET	field-effect transistor
FF	flip-flop
FILT	filter (VCF)
FIN	final
FINE	fine-tuning
FOA	(for Factory Use Only)
FREQ	frequency
FSK	frequency-shift keying
FT	foot
FTSW	footswitch
G	gate
GEN	generation, generator
GLD	glide
GND	ground
GRN	green
H, HEX	hexadecimal (base 16)
Hz	Hertz
I	inhibit
I	input (solid state switch)
Iabc	amplifier bias current (OTA CC)
IC	integrated circuit
IN	input
INIT	initial
INT	interrupt
INV	inversion, inverter
I/O	input/output
IRQ	interrupt request
J	jack (female pins)
JSTK	joystick
K	kilo-
KBD, KYBD	keyboard
L	lower
LD	load
LED	light-emitting diode
LFO	low frequency oscillator
LFT	left
LIM	limit, limiter
LIN	linear
LOG	logarithmic

LSB	least significant bit
LSI	large-scale integration
LVL	level
m	milli-
M	mega-
MAX	maximum
MEM	memory
MIN	minimum
MIX	mixer
MOD	modulation
MOS	metal-oxide semiconductor
MSB	most significant bit
MSI	medium-scale integration
MSUM	master summer
MTUN	master tune
MUX	multiplexing, multiplexer
n	nano-
NC	no connection
NC	normally closed contact
NEUT	neutral
NO	normally open contact
NOM	nominal
NORM	normal
NSE	noise
NVM	non-volatile memory
O	output (solid-state switch)
OBS	obsolete
OFST	offset
ORG	orange
OSC	oscillator (VCO)
OTA	operational transconductance amplifier
OUT	output
OV	overflow
p	pico-
P	plug (designator)
P-	polyphonic (modulation)
PBND	pitch bend
PC	program counter (in CPU)
PCB	printed circuit board
PED	pedal
PNK	pink
PNL	panel
POS	positive
POT	potentiometer
PR	pair
PRGM	program
PRGMR	programmer
PROM	programmable ROM
PRST	preset
PS	program select

PW	pulse width
PWM	pulse-width modulation
PWR	power
Q	transitor (designator)
QA	transistor array (designator)
QTY	quantity
R	resistor (designator)
RA	resistor array (designator)
RAM	random-access memory
REC	record
REF	reference
REG	regulation, regulator
REL	release
RES	resonance
REV	revision
RGT	right
RIP	ripple clock
ROM	read-only memory
RS	reset
RST	restart
S	switch
S	analog switch signal
SA	switch array (designator)
SAR	successive approximation register
SEC	second
SEL	select
SEQ	sequencer
SER	serial
S/H	sample and hold
SHT	sheet
SIG	signal
S/N	signal-to-noise ratio
S/N	serial number
SPAD	scratchpad (RAM)
SPK	spare parts kit
SPKR	speaker
SRAM	static RAM
SRC	source
SSI	smale-scale integration
ST	start
STRB	strobe
SUM	summation, summer
SUS	sustain
SYM	symmetry
SYNC	synchronization, synchronizer
SYNTH	synthesizer
SYS	system

T	transformer (designator)
TB	terminal board (designator)
TC	time constant
THRS	threshold
TP	test point (designator)
TRI	triangle-wave
TRIG	trigger
TRIM	trimming, trimmer
TTL	transistor-transistor logic
u	micro-
U	integrated circuit (designator)
U	upper
UART	universal asynchronous receiver-transmitter
ULSI	ultra-LSI
UNI	unison
USART	universal synchronous-asynchronous
V	Volts
V(A)	V supply, analog circuit
V(D)	V supply, digital circuit
V-C	voltage-to-current converter
VCA	voltage-controlled amplifier (AMP)
VCF	voltage-controlled filter (FILT)
VCO	voltage-controlled oscillator (OSC)
VDAC	DAC output voltage
VIOL	violet
VLSI	very-LSI
VMUX	POT MUX output voltage
V/OCT	volts-per-octave
VOL	volume
VPED	pedal voltage (or, voltage pedal)
VR	voltage regulator (designator)
VREC	voltage record
W	wiring or cable (designator)
W-	wheel (MOD)
WHT	white
XOR	exclusive-OR
Y	crystal (designator)
YEL	yellow

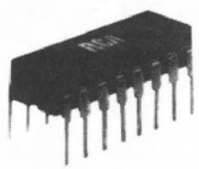
SECTION 8

APPENDIX

RCA
Solid State
Division

Linear Integrated Circuits
Monolithic Silicon
CA3280G, CA3280AG Types

File Number 1174



16-Lead Dual-In-Line
Plastic Package
With Hermetic Gold-CHIP
H-1622

Dual Variable Operational Amplifiers

"G" Suffix Type-Hermetic Gold-CHIP in Dual-In-Line Plastic Package

Features:

- **Low initial input-offset voltage: 500 μV max. (CA3280A)**
- **Low offset-voltage change versus I_{ABC}: $<$ 500 μV typ. for all types**
- **Low offset-voltage drift: 5 μV/C max. (CA3280A)**
- **Excellent matching of the two amplifiers for all characteristics**
- **Internal current-driven linearizing diodes reduce the external input current to an offset component**
- **Differential amplifier emitters brought out for use in emitter-coupled dual-differential amplifier applications**
- **Low noise: 8 nV/$\sqrt{Hz}$ @ 1 kHz typ.**
- **Low distortion: 0.4% THD typ.**
- **Two modes of gain control**
- **Hermetic Gold-CHIP in a plastic package**

The RCA-CA3280 and CA3280A types types consist of two variable operational amplifiers that are designed to substantially reduce the initial input offset voltage and the offset-voltage variation with respect to changes in programming current. This design results in reduced "AGC thump," an objectionable characteristic of many AGC systems. Interdigitation, or crosscoupling, of critical portions of the circuit reduces the amplifier dependence upon thermal and processing variables.

The CA3280 has all the generic characteristics of an operational voltage amplifier

(Continued on page 2)

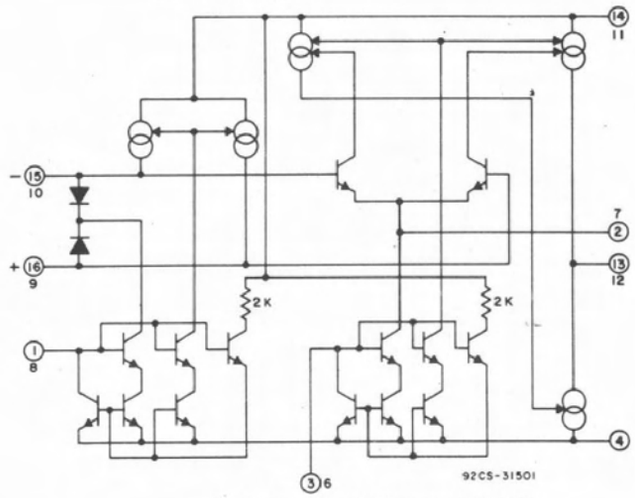


Fig. 1 – Functional diagram of 1/2 CA3280.

Printed in USA/3-79

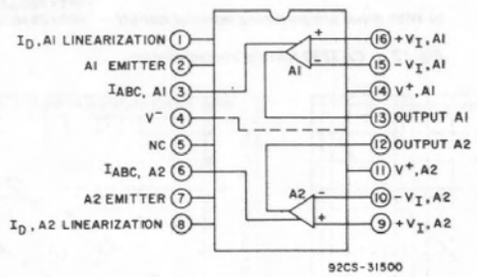
except that the forward transfer characteristic is best described by transconductance rather than voltage gain, and the output is current, not voltage. The magnitude of the output current is equal to the product of transconductance and the input voltage. This type of operational transconductance amplifier was first introduced by RCA in 1969*, and it has since gained wide acceptance as a gateable, gain-controlled building block for instrumentation and audio applications, such as linearization of transducer outputs, standardization of widely changing signals for data processing, multiplexing, instrumentation amplifiers operating from the nanopower range to high current and high-speed comparators.

* "OTA Obsoletes Op Amp," by C.F. Wheatley and H.A. Wittlinger, NEC Proceedings, December, 1969.

The CA3280 and CA3280A are supplied in the 16-lead dual-in-line Gold-CHIP plastic package (G suffix). The operating-temperature ranges are −55 to +125°C for the CA3280A, and 0 to +70°C for the CA3280. The CA3280 is also supplied as a hermetic Gold-CHIP (HG suffix).

Applications:

- **Voltage-controlled amplifiers**
- **Voltage-controlled filters**
- **Voltage-controlled oscillators**
- **Multipliers**
- **Demodulators**
- **Sample and hold**
- **Instrumentation amplifiers**
- **Function generators**
- **Triangle wave-to-sine wave converters**
- **Comparators**
- **Audio preamplifiers**

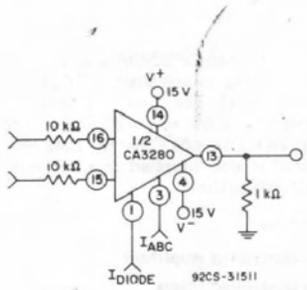


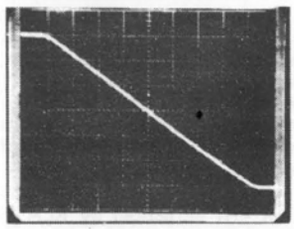
Terminal Assignment

MAXIMUM RATINGS, *Absolute-Maximum Values:*

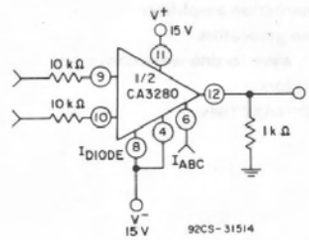
DC SUPPLY VOLTAGE (BETWEEN V^+ AND V^- TERMINALS)	36 V
DIFFERENTIAL INPUT VOLTAGE	±5 V
DC INPUT VOLTAGE RANGE	V^+ to V^-
INPUT SIGNAL CURRENT AT $I_D = 0$	100 μA
AMPLIFIER BIAS CURRENT	10 mA
OUTPUT SHORT CIRCUIT DURATION*	Indefinite
LINEARIZING DIODE BIAS CURRENT, I_D	5 mA
PEAK INPUT CURRENT WITH LINEARIZING DIODE	$\pm I_D$
POWER DISSIPATION, P_D:	
Either Amplifier	600 mW
Total Package	750 mW
Above 55°C	Derate linearly at 6.67 mW/°C
AMBIENT TEMPERATURE RANGE, T_A:	
Operating:	
CA3280	0 to +70°C
CA3280A	−55 to +125°C
Storage, All Types	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ±1/32 in. (1.59 ±0.79 mm) from case for 10 sec. max.	+265°C

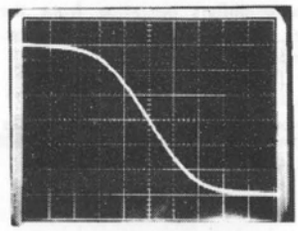
* Short circuit may be applied to ground or to either supply.





a) With diode programming terminal active





b) With diode programming terminal cut-off

Fig. 12 – CA3280 transfer characteristics.

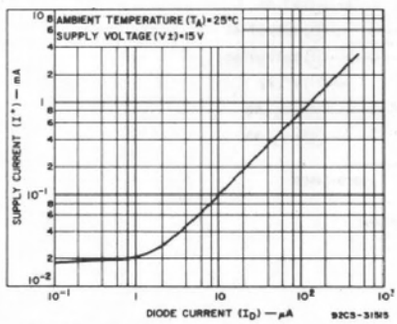


Fig. 13 – Supply current as a function of diode current.

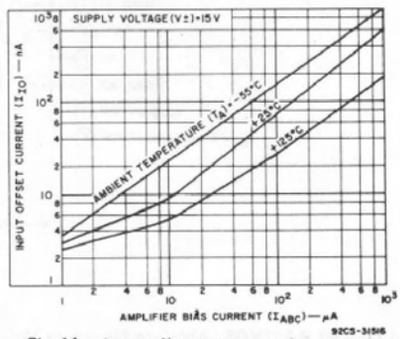


Fig. 14 – Input offset current as a function of amplifier bias current.

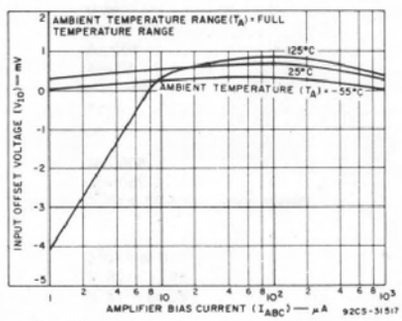


Fig. 15 – Input offset voltage as a function of amplifier bias current.

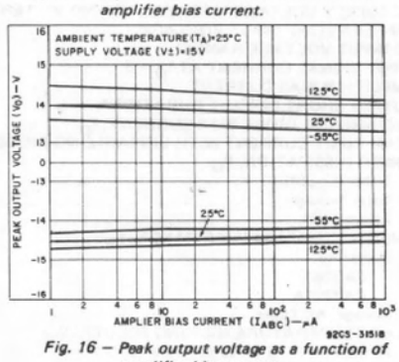


Fig. 16 – Peak output voltage as a function of amplifier bias current.

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CEM 3310

Voltage Controlled Envelope Generator

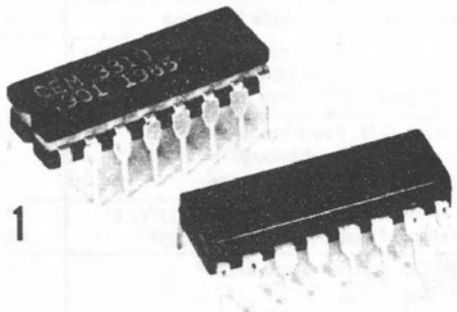
The CEM3310 is a self-contained, precision ADSR type of envelope generator intended for electronic music and other sound generation applications. Attack, decay and release times are exponentially voltage controllable over a wide range, and the sustain level is linearly voltage controllable from 0 to 100% of the peak voltage. A unique design approach allows for a 10,000 times improvement in control voltage rejection over conventional designs. In addition, much care has been given to the accuracy, repeatability and tracking of the parameters from unit to unit without external trimming. The times are to a first order determined only by the external resistor and capacitor and constant of physics, KT/q. Wide tolerance monolithic resistors are not used to set up the time constants or the control scale. Finally, all four control inputs are isolated from the rest of the circuitry so that the control pins of tracking units may be simply tied together. Although a low voltage process has been used to lower the cost and lower the leakage currents, an internal 6.5 volt Zener diode allows the chip to be powered by ± 15 volts supplies, as well as +15, -5 volt supplies.

* **Zero to -5V Varies the Times from 2mS to 20S**

** **Zero to +5V Varies the Sustain Level from 0 to 100%**

Features

- Low Cost
- Third Generation Design
- Large Time Control Range: 50,000 min
- Full ADSR Response
- True RC Envelope Shape
- Exceptionally Low Control Voltage Feedthrough: 90μV max
- Accurate Exponential Time Control Scales
- Isolated Control Inputs
- Good Repeatability and Tracking Between Units Without External Trim
- Independent Gate and Trigger
- ± 15 Volt Supplies



1

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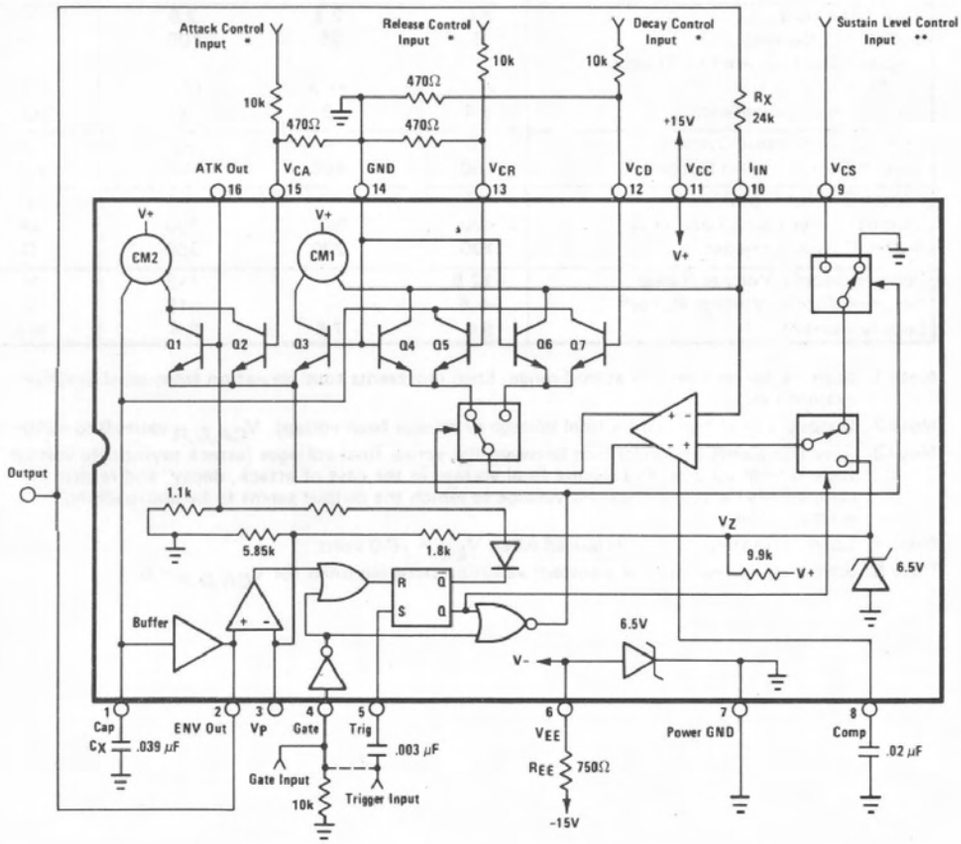
Circuit Block and Connection Diagram



CEM 3310

Electrical Characteristics

V_{CC} = +15.0V V_{EE} = -5.0 to -15.0V R_X = 24K T_A = 25°C				
	MIN	TYP	MAX	Units
Time Control Range	50,000:1	250,000:1	–	
Attack Asymtote Voltage (V_Z)	6.1	6.5	6.9	V
Attack Peak Voltage (V_p)	4.7	5.0	5.3	V
Attack Peak to Asymptote Tracking	–	1.5	4	%
Control Scale Sensitivity	58.5	60	61.5	mV/Decade
Temperature Coefficient of Control Scale	+3,000	+3,300	+3,600	ppm
ATK, DCY, RLS Scale Tracking	-300	0	+300	μV/Decade
Exponential Full Scale Control Accuracy[1]				
50nA < I_O < 50 μA	–	0.3	1.5	%
2nA < I_O < 200 μA	–	2	10	%
Attack C.V. Feedthrough[2]	–	6	90	μV
Decay C.V. Feedthrough[2]		NONE		
Release C.V. Feedthrough[2]		NONE		
Sustain Final Voltage Error (V_O-V_{CS})	-3	+10	+23	mV
Release Final Voltage Error (V_O)	-3	+10	+23	mV
RC Curve Asymptote Error[3]				
$V_{CA,D,R}$ = 0	–	-6	-60	μV
$V_{CA,D,R}$ = -240mV	–	-125	-1250	mV
Input Current (I_{IN}) to Output Current (I_O) Ratio, $V_{CA,D,R}$ = 0.[5]				
Charge Current (ATK)	.75	1	1.3	
Discharge Current (DCY, RLS)	.83	1	1.2	
Buffer Input Current (I_{B2})	–	0.5	5	nA
Op Amp Input Current (I_{B1})	150	400	800	nA
Gate Threshold	2.0	2.3	2.6	V
Gate Input Current	5	25	100	μA
Trigger Pulse Required to Trigger Envelope	+1.1	+1.3	+1.5	V
Trigger Input Impedance	2.4	3	4	KΩ
Time Control Input Current	0.5	–	2500	nA
Sustain Control Input Current	150	400	800	nA
Attack Output Signal	-.4	-.8	-1.2	V
Output Current Sink Capability	420	560	700	μA
Buffer Output Impedance	100	200	350	Ω
Positive Supply Voltage Range	+12.5	–	+18	V
Negative Supply Voltage Range[4]	-4.5	–	-18	V
Supply Current	5.6	7.5	9.4	mA

Note 1: Scale factor determined at mid-range. Spec represents total deviation from ideal at range extremities.

Note 2: Output is at either sustain final voltage or release final voltage. $V_{CA,D,R}$ varies 0 to -240mV.

Note 3: Spec represents the difference between the actual final voltages (attack asymptote voltage, sustain final voltage, and release final voltage in the case of attack, decay, and release respectively) and the apparent voltage to which the output seems to be approaching asymptotically.

Note 4: Current limiting resistor required when V_{EE} > -6.0 volts.

Note 5: Spec also represents time constant variation between units for $V_{CA,D,R}$ = 0.

Application Hints

Supply

Since the device can withstand no more than 24 volts between its supply pins, an internal 6.5 volt ± 10% zener diode has been provided to allow the chip to run off virtually any negative supply voltage. If the negative supply is between -4.5 and -6.0 volts, it may be connected directly to the negative supply pin (pin 6). For voltages greater than -7.5 volts, a series current limiting resistor must be added between pin 6 and the supply. Its value is calculated as follows:

$$R_{EE} = (V_{EE} - 7.2)/.010.$$

The circuit was designed for a positive supply of +15 volts. Voltages other than +15 volts will cause the peak threshold voltage to be either at a minimum of .33V_{CC} or at a maximum of 5.5 volts.

Gate and Trigger Inputs

The gate input is referenced to ground and therefore will accept any ground referenced TTL or CMOS logic level up to +18 volts. If the gate pin is left floating, it will be interpreted as a high level. The trigger input is referenced to the V_{EE} pin (pin 6) and therefore, a ground referenced trigger pulse should be capacitively coupled to the trigger input pin (pin 5).

Input Control Voltages

As the scale sensitivity on the three time control inputs is 60mV/decade, attenuation of the incoming control voltages will in most cases be required. Four decades of control requires only a 240mV voltage excursion. The more negative the voltages the longer the times. For best scale accuracy at the shortest times, the impedance at the time control pins should be kept low. At the shortest times (corresponding to 200 μA of peak

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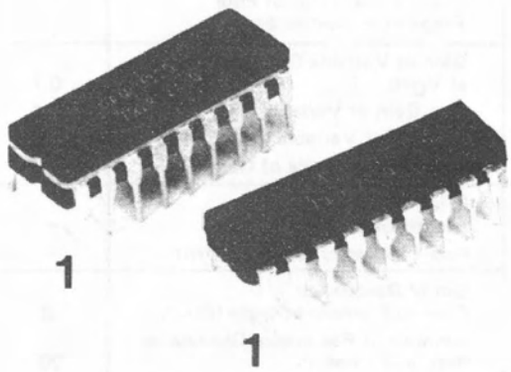
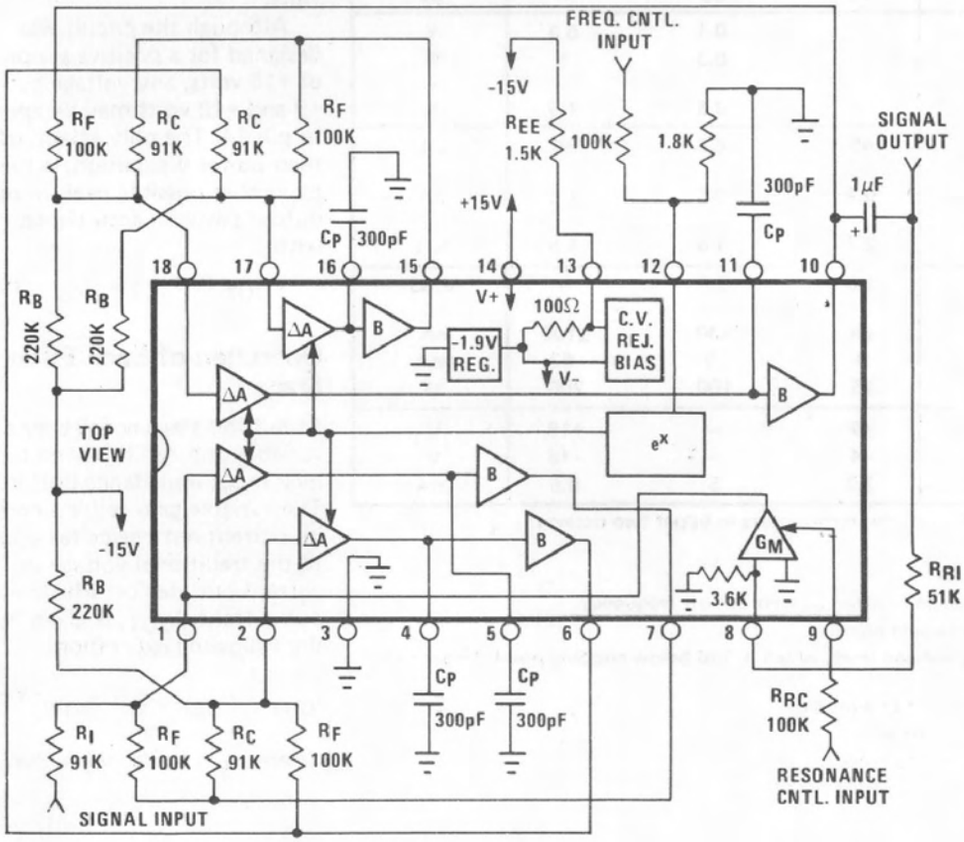
CEM 3320

Voltage Controlled Filter

The CEM 3320 is a high performance voltage controlled four-pole filter complete with on-chip voltage controllable resonance. The four independent sections may be interconnected to provide a wide variety of filter responses, such as low pass, high pass, band pass and all pass. A single input exponentially controls the frequency over greater than a ten octave range with little control voltage feedthrough. Another input controls the resonance in a modified linear manner from zero to low distortion oscillation. For those demanding applications, provision has been made to allow trimming for improved control voltage rejection. Each filter section features a novel variable gain cell which, unlike the traditional cell, is fully temperature compensated, exhibits a better signal-to-noise ratio and generates its low distortion predominantly in the second harmonic. The device further includes a minus two volt regulator to ensure low power dissipation and consequent low warm-up drift even with ±15 volt supplies.



Circuit Block and Connection Diagram



Features

- Low Cost
- Voltage Controllable Frequency: 12 octave range minimum
- Voltage Controllable Resonance: From zero to oscillation
- Accurate Exponential Frequency Scale
- Accurate Linear Resonance Scale
- Low Control Voltage Feedthrough: -45dB typical
- Filter Configurable into Low Pass, High Pass, All Pass, etc.
- Large Output: 12V.P.P. typical
- Low Noise: -86dB typical
- Low Distortion in Passband: 0.1% typical
- Low Warm Up Drift
- Configurable into Low Distortion Voltage Controlled Sine Wave Oscillator
- ±15 Volt Supplies

CEM 3320

Electrical Characteristics

V_{CC} = +15V,	R_F = 100K	T_A = 25°C		
Parameter	Min.	Typ.	Max.	Units
Pole Frequency Control Range	3500:1	10,000:1	–	•
Sensitivity of Pole Frequency Control Scale, Midrange	57.5	60	62.5	mV/decade
Tempco of Pole Frequency Control Scale	3000	3300	3600	ppm
Exponential Error of Pole Frequency Control Scale[1]	–	4	12	%
Gain of Variable Gain Cell at V_C=0	0.7	0.9	1.3	
Max Gain of Variable Gain Cell	2.4	3.0	3.6	
Tempco of Variable Gain Cell[2]	–	500	1500	ppm
Output Impedance of Gain Cell[2]	0.5	1.0	2.0	MΩ
Pole Frequency Control Feedthrough	–	60	200	mV
Pole Frequency Warm-up Drift	–	.5	1.5	%
Gm of Resonance Control Element at I_{CR}=100uA	.8	1.0	1.2	mmhos
Amount of Resonance Obtainable Before Oscillation	20	30	–	dB
Resonance Control Feedthrough[3]	–	0.2	1.5	V
Output Swing At Clipping	10	12	14	V.P.P.
Output Noise re Max Output[4]	-76	-86	–	dB
Rejection in Bandreject	73	83	–	dB
Distortion in Passband[5,7]	–	0.1	0.3	%
Distortion in Bandreject[6,7]	–	0.3	1	%
Distortion of Sine Wave Oscillation[8]	–	0.5	1.5	%
Internal Reference Current, I_{REF}	45	63	85	μA
Input Bias Current of Frequency Control Input	0.2	0.5	1.5	μA
Input Impedance to Resonance Signal Input	2.7	3.6	4.5	KΩ
Buffer Slew Rate	1.5	3.0	–	V/uS
Buffer Input Bias Current (I_{EE}=8mA)	±8	±30	±100	nA
Buffer Sink Capability	.4	.5	.63	mA
Buffer Output Impedance[2]	75	100	200	Ω
Positive Supply Range	+9	–	+18	V
Negative Supply Range[9]	-4	–	-18	V
Positive Supply Current	3.8	5	6.5	mA

Note 1: -25mV < V_C < +155mV. Most of this error occurs in upper two octaves.

Note 2: V_C = 0

Note 3: Untrimmed. 0 < I_{CR} < 100μA

Note 4: Filter is connected as low pass and set for 20 KHz cut-off frequency.

Note 5: Output signal is 3dB below clipping point.

Note 6: Output signal is 3dB below passband level, which is 3dB below clipping point. In general, this is worst case condition.

Note 7: Distortion is predominantly second harmonic.

Note 8: Sinewave is not clipped by first stage.

Note 9: Current limiting resistor always required.

Application Hints

Supplies

In order to minimize the power dissipation, the negative supply is regulated at -1.9 volts with an internal shunt regulator. This not only reduces warm-up drift of the pole frequencies at power turn-on, but also allows virtually any negative supply greater than -4 volts to be used. The current limiting resistor, R_{EE}, must always be included and is calculated as follows:

$$R_{EE} = \frac{V_{EE} - 2.7V}{0.008}$$

As can be seen from the Block Diagram, an internal 100Ω resistor is in series between the regulator and pin 13. This resistor, which allows for trimming of the control voltage feedthrough (explained in further detail below) results in an actual voltage at pin 13 of around -2.7 volts.

Although the circuit was designed for a positive supply of +15 volts, any voltage between +9 and +18 volts may be applied to pin 14. The only effect, other than power dissipation, is the maximum possible peak-to-peak output swing in accordance with:

$$V_{OUT}\ (V.P.P.) = V_{CC} - 3V$$

Operation of Each Filter Stage

Each filter stage consists of a variable gain cell followed by a high input impedance buffer. The variable gain cell is a current-in, current-out device (as opposed to the traditional voltage-in, current-out device) whose output current, I_{OUT}, is given by the following expression:

$$I_{OUT} = (I_{REF} - I_{IN})\ A_{IO}\ e^{-V_C/V_T}$$

where V_T = KT/q, V_C is the

Absolute Maximum Ratings

Voltage Between V_{CC} and V_{EE} Pins	+22V,-0.5V
Voltage Between V_{CC} and Ground Pins	+18V,-0.5V
Voltage Between V_{EE} and Ground Pins	-4V,+0.5V
Voltage Between Cell Input and Ground Pins	+0.5V,-6V
Voltage Between Frequency Control and Ground Pins	±6V,
Voltage Between Resonance Control and Ground Pins	+2V,-18V
Current Through Any Pin	±40mA
Storage Temperature Range	-55° C to +150° C
Operating Temperature Range	-25° C to +75° C

voltage applied to pin 12, A_{IO} is the current gain of the cell at V_C = 0 (Nominally 0.9), and

$$I_{REF} = \frac{.46V_{CC} - .65V}{100K^*}$$

*±25%

As the input to the variable cell is a forward biased diode to ground, it presents essentially a low impedance summing node at a nominal 650mV above ground. The required input currents may therefore be obtained with resistors terminating at this input node.

For normal operation of any filter type, each stage is set up with a feedback resistor, R_F, from the buffer output to the variable gain cell input, and with the pole capacitor, C_P, connected to the output of the variable gain cell. This setup is shown in Figure 1. In the D.C. quiescent state, the buffer output will always adjust itself so that a current equal to I_{REF} flows into the input.

For lowest control voltage feedthrough and maximum peak-to-peak output signal, the quiescent output voltage of each buffer, V_{ODC}, should be:

$$V_{ODC} = .46V_{CC}$$

Thus, in the simple case of Figure 1, R_F is calculated as follows:

$$R_F = \frac{V_{ODC} - .65V}{I_{REF}}$$

$$= 100K \text{ nominal}$$

Since I_{REF} can vary ±25%, V_{ODC} can vary nearly 30% from device to device using a standard 5% resistor for R_F. In the typical case where V_{CC} = +15V, I_{REF} is 63μA nominal, and the D.C. output of each buffer should be set for +6.9V nominal.

The output impedance of the variable gain cell, although high, has a finite value. This impedance is reflected back to the input as an A.C. resistance of nominally 1 megohm in parallel with the feedback resistor, R_F, regardless of control voltage value. The pole frequency of each filter section is determined by the total equivalent feedback resistance, R_{EQ}, and the pole capacitor in the expression:

$$f_P = \frac{A_{IO}}{2\pi R_{EQ} C_P} e^{-V_C/V_T}$$

where:

$$R_{EQ} = \frac{R_F \cdot 1M\Omega^*}{R_F + 1\,M\Omega^*}$$

*-50%, +100%

Signal Coupling into a Filter Section

For the filter section to provide the low pass function, the input signal is coupled via a scaling resistor, R_C, into the input. If the signal is the external input to the entire filter, it will in general have a D.C. quiescent voltage level of zero, and all of I_{IN} equal to I_{REF} for the first stage will be provided by its feedback resistor. If the signal is from the output of a previous filter section, it will have a quiescent level of .46V_{CC} (6.9 volts for a +15 volt supply). Therefore, part of I_{IN} will be supplied by this voltage through R_C while the remainder will be sourced through R_F.

The voltage gain in the passband is given by R_{EQ}/R_C. In general, this gain should be set to unity for stages two, three and four. The input resistor to stage one can be scaled for any size of the external input signal. The resistance value should be selected so that the maximum external input signal produces the maximum passband output signal before clipping.

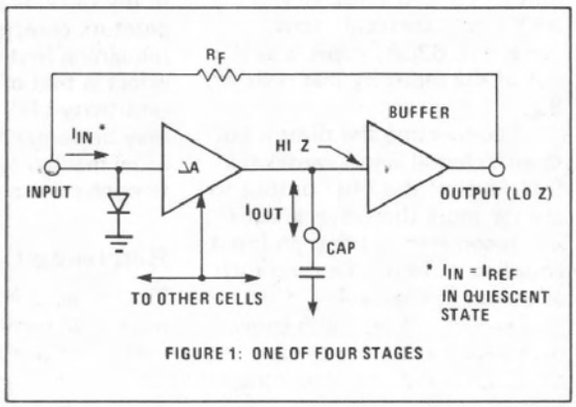


FIGURE 1: ONE OF FOUR STAGES

To generate the hi-pass function, the input signal is coupled into the variable gain element output via the pole capacitor, C_P. Therefore, any D.C. voltage level is blocked by the capacitor and I_{IN} equal to I_{REF} for each input is supplied only through the feedback resistors. The voltage gain in the pass band is simply unity, regardless of the value of R_F. For best results, the output impedance of whatever is generating the external input signal to stage one should be low compared to $R_F/4$.

Sample Filter Circuits

The Block Diagram shows the external components connections for a four-pole, low-pass filter designed to operate off ±15 volt supplies. The values for R_F, R_C, and R_B were chosen so that a) when the 1 megohm reflected resistance is in parallel with R_F, the gain of stages two, three and four is unity, and b) with the buffer outputs at the proper quiescent level of 6.9 volts, the total current into each input is the required 63μA. For stage 1, all of this quiescent current is sourced by the feedback resistor. For stages two, three, and four, 63μA is sourced by the feedback resistor, while 70μA is sourced by the coupling resistor for a total sourced current of 133μA. Thus, to end up with a net quiescent input current of 63μA, 70μA is sunk out of the input by bias resistor, R_B.

If connecting the filter input to an external signal causes the D.C. level of the filter output to change more than several volts, it is recommended that an input coupling capacitor be used such as shown in Figure 4.

Figures 2, 3, 4, and 5 show high-pass, band-pass, all-pass, and state variable realizations, all with the voltage controlled resonance feature. Note that due to the configuration of the resonance feedback, the resonance frequency of the high-pass will be approximately 2.4 times higher than that of the low-pass, while the resonance frequency of the band-pass and all-pass will be 1/2.4 = .42 times lower than that of the low-pass, for the same component values. For the state variable, resistor R_Q adds positive feedback to increase the maximum Q, which is otherwise limited by the reflected 1MΩ impedance across the integrators.

Pole Frequency Control Scale

The current gains of each of the four sections (and consequently their pole frequencies) are controlled simultaneously with a voltage applied to pin 12. Since the scale is exponential with the standard 18mV/octave (60mV/decade), an input attenuator network will in most cases be required. An increasing positive control voltage lowers the pole frequencies of the filter. For best results over a thousand-to-one control range, the voltage on pin 12 should be maintained between -25mV and +155mV.

Unlike the typical variable transconductance cell used in most V.C. filters, the four stages in the CEM 3320 are fully temperature compensated. The only remaining first order temperature effect is that of control scale sensitivity ($1/V_T$). This effect may be compensated in the usual manner with a +3300ppm tempco resistor (Tel Labs Q81).

Resonance Control

The variable gain cell used to control the amount of resonance is the traditional transconductance type of amplifier. It has a separate signal voltage input (pin 8), a separate control current input with a modified linear scale (pin 9), and a current output internally connected to the input of stage one. With an impedance of 3.6K ±900Ω, the input is referenced to ground; thus, connection to the filter output will require a coupling capacitor.

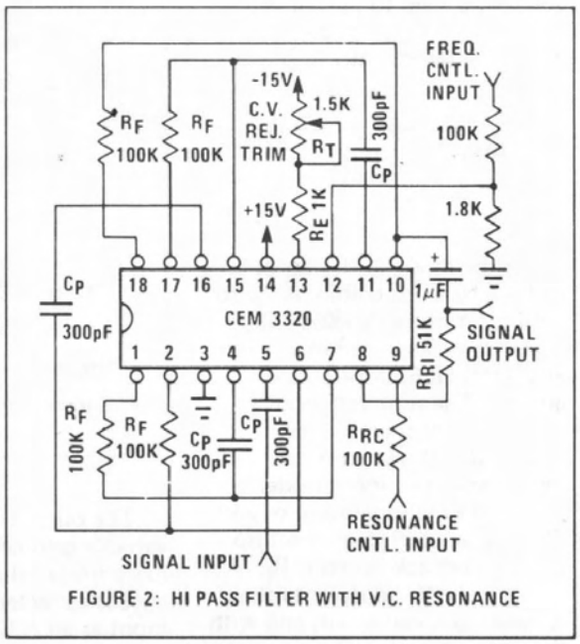


FIGURE 2: HI PASS FILTER WITH V.C. RESONANCE

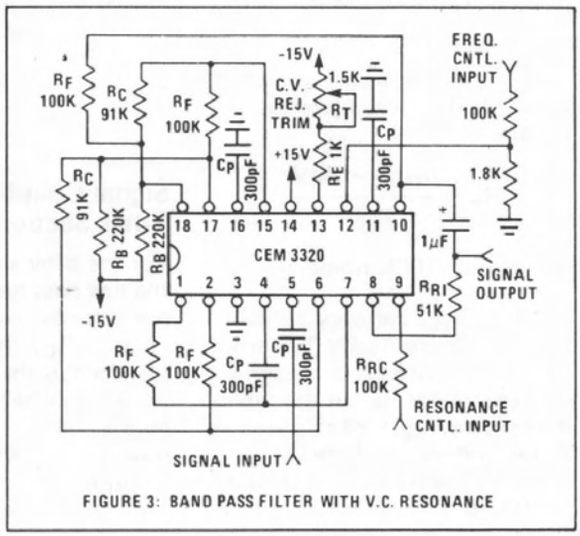


FIGURE 3: BAND PASS FILTER WITH V.C. RESONANCE

Control of the transconductance is accomplished with a current input. As the control input is a low impedance summing node at a potential near ground, the control current may be derived from the resonance control voltage with an input resistor, R_{RC}, terminated at pin 9. This resistor should be selected so that the maximum available resonance control voltage produces the maximum desired control current.

Figure 6 shows a graph of the transconductance versus control current. As can be seen, the slope of the curve becomes more gradual as the control current increases. This feature allows the resonance to be controlled with finer resolution as the critical point of oscillation is approached.

The maximum control current is therefore selected in accordance with the amount of control sensitivity which is desired at the top of the control range. The value of the input resistor, R_{RI}, is then selected depending on where in the control scale oscillation is desired to begin (when the control voltage is 90% of the maximum value, for instance). The following formula may be used:

$$R_{RI} = 3.6K^{*} \left(\frac{Gm_{OSC}\, R_{EQ} - 1}{A_{OSC}}\right)$$

*±25%

where Gm_{OSC} is the transconductance corresponding to the control current at which oscillation is desired to begin; and where A_{OSC} is the overall gain from the resonance signal input resistor, R_{RI}, to the filter output required to sustain oscillation. If the gain of stages 2, 3 and 4 are unity, then A_{OSC} = 12dB or 4 in the case of the low pass filter.

While operating the filter in the resonant mode, care should be taken not to overload the input to the filter. If the signal output of stage one is allowed to become clipped, then not only will the apparent resonance of the signal at the filter output appear to be reduced, but the D.C. level of the output signal will shift.

When the resonance control is advanced until sustained oscillations are produced, advancing the resonance control further will merely increase the amplitude of the oscillation. A lesser effect is the shift of the oscillation frequency. For minimum shift (typically less than 0.5%), the oscillation amplitude should be kept below the clipping level of the first stage output. Allowing the oscillation to be clipped will produce frequency shifts in excess of 5%.

Other Uses of the Resonance Control Cell

Other than controlling the resonance, the variable transconductance amplifier may be used as an independent VCA controlling the amplitude of the input signal to the filter. Or the cell may be set up as a symmetrical limiter/clipper for either preventing large dynamic input signals from overloading the filter or for providing additional coloration to the input signal.

Pole Frequency Control Voltage Rejection

The D.C. voltage shift at the filter output due to the frequency control voltage may be minimized by adjusting the current into the minus supply pin, pin 13. This is accomplished by replacing the negative supply current limiting resistor, R_{EE},

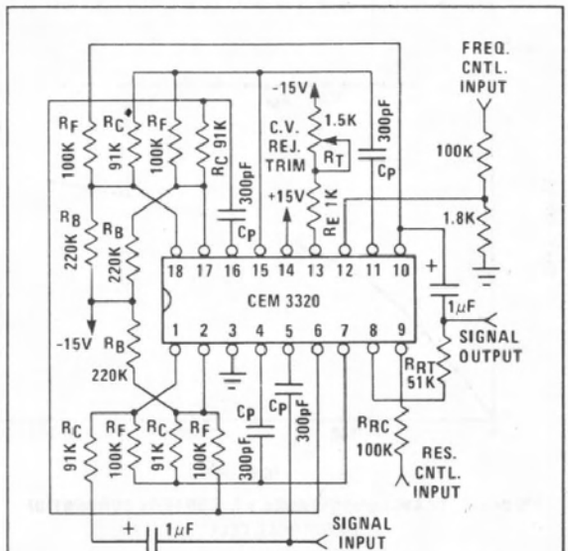


FIGURE 4: ALL PASS FILTER WITH V.C. RESONANCE

with a series resistor and trim pot. The fixed resistor, R_E, and series trim pot, R_T, should be selected so that the current into pin 13 may be adjusted from 5mA to 12mA. Or:

$$R_E = \frac{V_{EE} - 3.2V}{12mA}$$

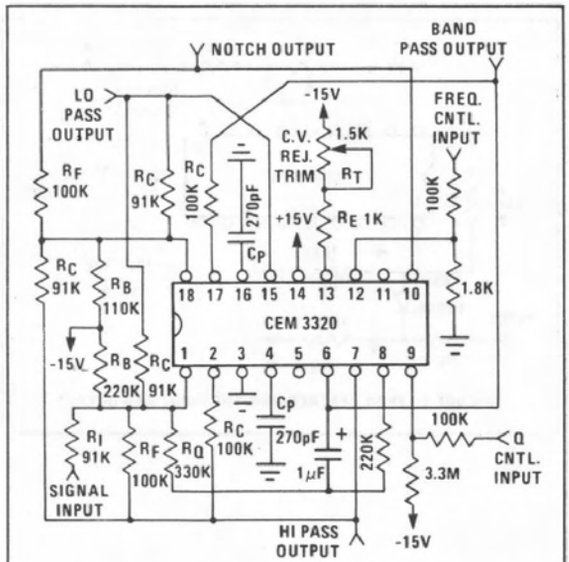


FIGURE 5: STATE VARIABLE FILTER WITH V.C. "Q"

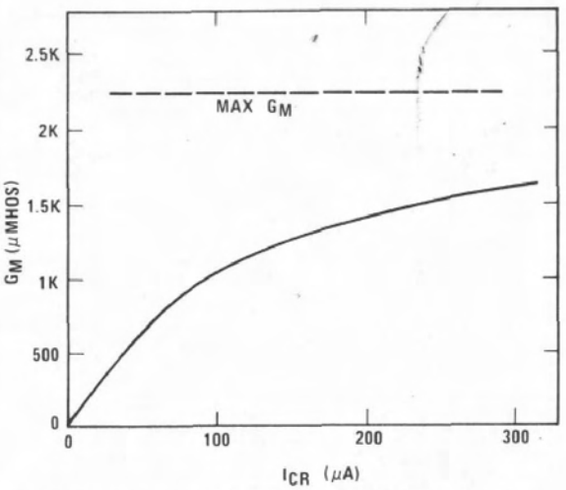


FIGURE 6: TRANSCONDUCTANCE V.S. CONTROL CURRENT OF RESONANCE CELL

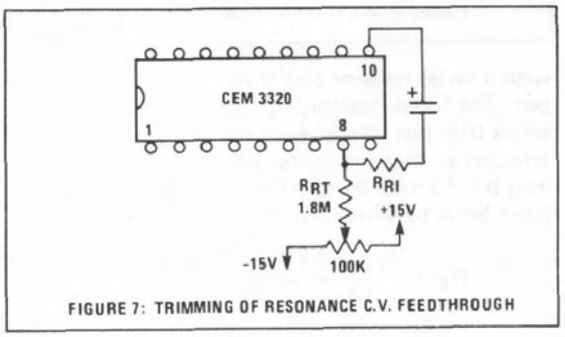


FIGURE 7: TRIMMING OF RESONANCE C.V. FEEDTHROUGH

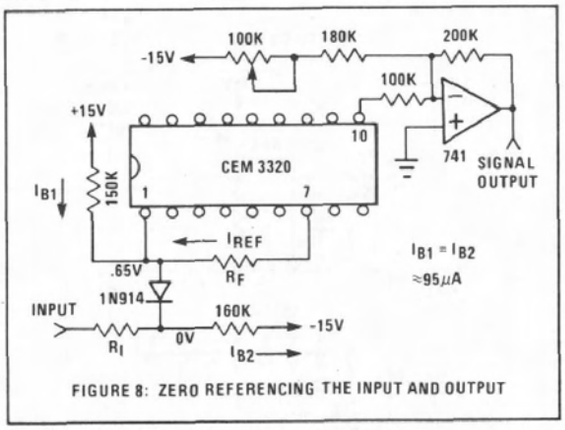


FIGURE 8: ZERO REFERENCING THE INPUT AND OUTPUT

and

$$R_T = \frac{V_{EE} - 2.4V}{5mA} - R_E$$

These components are shown in the filter circuits of Figures 2-5. To obtain minimum control voltage feedthrough, the best technique for adjusting this trim is to switch back and forth between the maximum and minimum control voltages while adjusting the pot so that the D.C. output voltage at these two extreme conditions is the same.

Resonance Control Voltage Rejection

For most applications, no trimming should be necessary. However, if required, the resonance control voltage feedthrough may be minimized by applying a small D.C. voltage on the resonance signal input pin, pin 8. A typical set-up is shown in Figure 7. The value of R_{RT} should be selected so the trim pot is able to adjust the voltage on pin 8 by ± 30mV.

Stage Buffers

Each buffer can source up to 10mA and sink a nominal 500μA. However, any D.C. load greater than ±200μA to ±300μA may begin to degrade the performance of the filter, especially if the loads on each buffer differ by more than this amount. The maximum recommended D.C. loads are 1mA source, 250μA sink, and a 150μA load difference between buffers. The maximum recommended A.C. loads are ±250μA.

Since the D.C. level at the filter output is at some non-zero voltage (6.9 volts for V_{CC} = +15V), a coupling capacitor will be required somewhere in the signal chain, either at the filter output or the following device inputs. Note that if the resonance feature is being used, the filter output is already D.C. blocked by the resonance input coupling capacitor, thus providing a convenient output point. If D.C. coupling to ground referenced inputs and outputs is required, the schemes shown in Figure 8 may be used. Note that the output circuit has the benefits of 1) allowing for gain after the filter, and 2) providing an output with greater drive capability. The buffer outputs are not short circuit protected; therefore care should be exercised to not short the outputs to ground or either supply.

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Absolute Maximum Ratings

Voltage Between V_{CC} and V_{EE} Pins	24V
Voltage Between V_{CC} and Ground Pins	+18V
Voltage Between V_{EE} and Ground Pins	-6.0V
Current Into V_{EE} Pin	±50mA
Voltage Between Control and Ground Pins	±6.0V
Voltage to Gate and Trigger Input Pins	V_{EE} to V_{CC}
Storage Temperature Range	-55°C to +150°C
Operating Temperature Range	-25°C to +75°C

current), every 100Ω will cause a 1% increase in control scale error. As the times are increased, this error will decrease in direct proportion.

The voltage applied to the sustain level control input will directly determine the sustain voltage of the output envelope (minus the sustain final voltage error). Voltages greater than the threshold voltage will cause the envelope to ramp up to this higher voltage when the peak threshold is reached. The rate at which this occurs will be equal to the fastest attack rate.

Since all four control inputs are connected only to the bases of NPN transistors, the control input pins of tracking units may be simply tied together. Therefore, in the case of the time control inputs, only one attenuator network is required to control the same parameter in a multiple chip system.

Selection of R_X and C_X

As is shown in the envelope equations, the RC time constant of the attack, decay and release curves is given by R_XC_X times the exponential multiplier, $\exp(-V_C/V_T)$. Practical circuit limitations determine R_X and the multiplier, from which C_X can then be calculated. The peak capacitor charging and discharging currents is given by $(V_Z/R_X)\exp(V_{CA}/V_T)$, $(V_{CS}/R_X)\exp(V_{CD}/V_T)$, and $(V_P/R_X)\exp(V_{CR}/V_T)$ for the attack, decay, and release phases respectively. For the best scale accuracy and tracking at the shortest times, these currents should be kept less than 100 μA, and in all cases they should not be allowed to exceed 300 μA. This sets the minimum value for R_X at 24K. Larger values of R_X will allow positive time control voltages to be used. However, as can also be seen from the envelope equations, the sustain/final voltage error, the asymptote error, and the control voltage feedthrough are all affected by R_X. A practical maximum of 240K is recommended for R_X when the internal buffer is used and 1M if an external FET buffer is used.

Trimming the Envelope Times

The RC time constants of the output envelope will typically track to within ± 15% from unit to unit, even at the longest time settings. If better tracking is required, the best method for trimming the time constants is to simply adjust R_X with a trimming potentiometer.

Output Drive Capability

The buffer output can sink at least 400 μA and can source up to 10mA, but with considerable degradation in performance. An output load no less than 20K to ground is recommended.

The buffer has a somewhat high output impedance. As a result of this, small steps (50mV) appear in the output waveform at the phase transitions, due to the sudden change in drive the output must provide to R_X. The largest step is at the beginning of the envelope and is given by $(R_O/R_X)V_Z$. It may be decreased by increasing R_X, lowering R_O, or using an external buffer with a low output impedance. R_O may be lowered by adding a resistor from the output pin to V_{EE}. However, every 1mA of current drawn from the output pin may increase the buffer input current as much as 5-6 nA with consequent degradation in performance.

Envelope Equations

Attack Curve

$$V_{OA} = V_Z\,(1-\exp(-\frac{t}{R_XC_X}\,e^{V_{CA}/V_T}))$$

Decay Curve

$$V_{OD}=(V_P-V_{CS})\exp(-\frac{t}{R_XC_X}\,e^{V_{CD}/V_T})+V_{CS}$$

Release Curve

$$V_{OR} = V_{CS}\exp(-\frac{t}{R_XC_X}\,e^{V_{CR}/V_T})$$

Sustain/Release Final Voltage Error

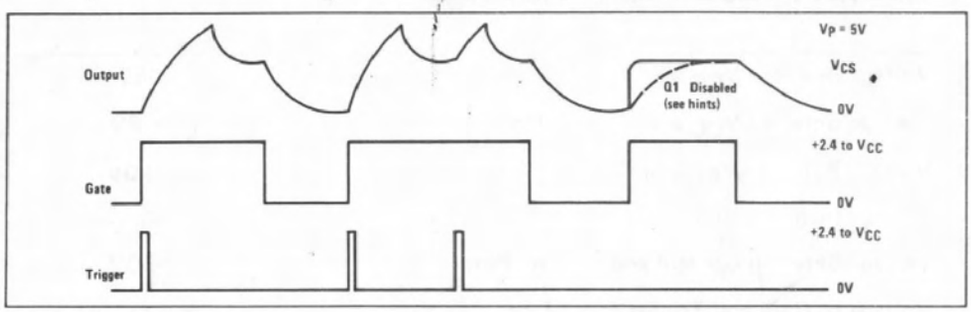
$$\epsilon_F = V_{OS} + I_{B1}R_X - I_{B2}R_X/1+e^{V_{CA}/V_T}$$

Attack/Decay/Release Asymptote Error

$$\epsilon_A = V_{OS} + I_{B1}R_X - I_{B2}R_X\,e^{-V_{CA,D,R}/V_T}$$

V_{CA} = Attack Control Voltage
V_{CD} = Decay Control Voltage
V_{CR} = Release Control Voltage
V_{CS} = Sustain Control Voltage
V_{OS} = Op Amp Offset
I_{B1} = Op Amp Input Current
I_{B2} = Buffer Input Current
V_Z = Attack Asymptote Voltage
V_P = Envelope Peak Voltage
V_T = kT/q

Input and Output Waveforms



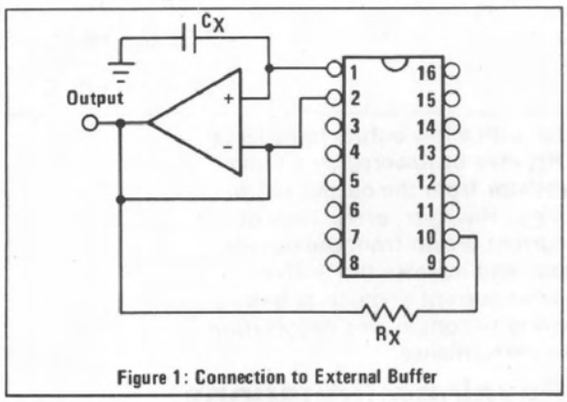


Figure 1: Connection to External Buffer

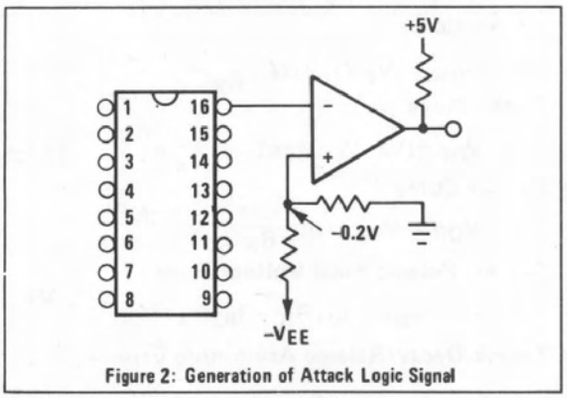


Figure 2: Generation of Attack Logic Signal

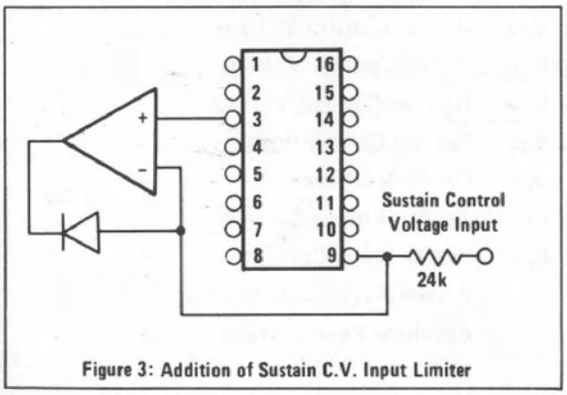


Figure 3: Addition of Sustain C.V. Input Limiter

Use of External Buffer

For various reasons, it may be desired to use an external buffer. One possible benefit might be a lower input bias current (I_{B2}), with consequent improvement in the associated errors. The external buffer should be connected as shown in Figure 1. For proper operation, the buffer used should be capable of sourcing at least 700 μA and should have a positive current flowing into the input pin, such as that resulting from NPN or P channel JFET inputs.

Disabling the Control Voltage Rejection Circuit

The purpose of Q1 (see block diagram) is to greatly reduce the control voltage feedthrough. During the attack phase, the base of Q1 is brought negative effectively disabling it and allowing Q2 to control the charging current. During the decay and release phases, however, the base of Q1 is at ground, causing negative voltage excursions on the base of Q2 to vary the charging current only a maximum of 2:1 (as opposed to the normal 10,000:1 or greater). Under normal triggering conditions (applying a trigger and a gate), this has no consequence, except to reduce the attack control voltage feedthrough to a negligible amount. However, if only a gate is applied with no trigger, the output will ramp up to the sustain level, approaching it asymptotically with a RC time constant of $R_XC_X(\exp(V_{CA}/V_T) + 1)$ (i.e. a rapid attack with only a 2:1 control range). To provide the normal full range of attack control under this mode of operation, Q1 should be disabled by connecting a resistor from pin 16 to V_{EE} to generate at least –500mV at the base of Q2. This resistance may be calculated as follows:

$$R = 1100(2V_{EE}-1)$$

The result will be 5,000 times or more sustain and release final voltage shift with the attack control voltage. If external circuitry is added to apply the –500 mV only when the gate is high, then only the sustain final voltage will exhibit significant shift.

Use of the Attack and Threshold Voltage Output Pins

The attack output pin (pin 16) and the peak threshold voltage pin (pin 3) have been provided to allow additional flexibility. Since pin 16 outputs a –.4 to –1.2 volts only during the attack phase, it may be used to provide a logic signal which indicates the attack phase (see figure 2). This signal may be ANDed with the gate to provide a logic signal indicating the decay phase. As was mentioned above, a sustain control voltage greater than the threshold voltage will result in a "jump" to the sustain level. By using the threshold voltage pin as shown in figure 3, the sustain voltage can be prevented from rising above the envelope peak, thus eliminating this undesirable effect. (This effect can also be eliminated by disabling the control voltage rejection circuit as described above).

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CEM 3340 / 3345

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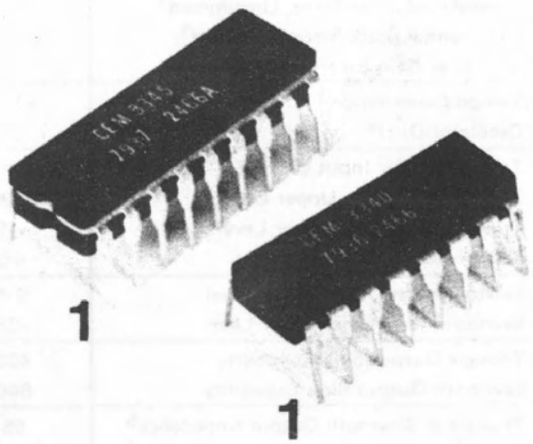
Voltage Controlled Oscillator

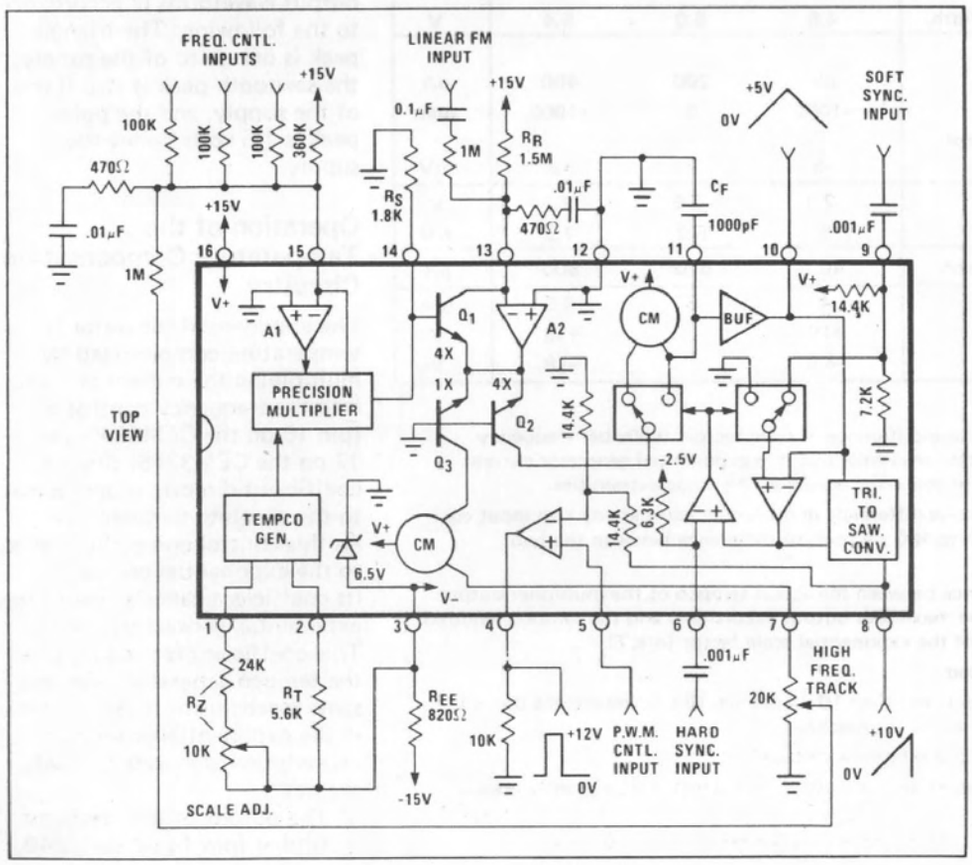
The CEM 3340 and CEM 3345 are completely self contained, precision voltage controlled oscillators, featuring both exponential and linear control scales and up to four buffered output waveforms: triangle, sawtooth, square, and pulse with voltage controllable pulse width. Full temperature compensation makes these VCOs extremely stable, and eliminates the need for a temperature compensation resistor. The highly accurate exponential and linear control inputs are virtual ground summing nodes, allowing multiple control voltages to be mixed within the device itself.

Also included is provision for hard and soft synchronization of the frequency, and an output for easy adjustment of high frequency tracking. Special care in the design ensures oscillation start-up under any power-on sequence and supply conditions.

Although a low voltage process has been used to reduce die size, cost, and leakage currents, an on-chip 6.5 volt zener diode allows the device to operate off ±15 volt supplies, as well as +15,-5 volt supplies.



CEM 3340 Circuit Block and Connection Diagram



Features

- Large Sweep Range: 50,000:1 min.
- Fully Temperature Compensated; No Q81 Resistor Required
- Four Output Waveforms Available; No waveform trimming required.
- Summing Node Inputs for Frequency Control
- High Exponential Scale Accuracy
- Low Temperature Drift
- Voltage Controlled Pulse Width
- Hard and Soft Sync Inputs
- Linear FM
- Buffered, Short Circuit Protected Outputs
- ±15 Volt Supplies

CEM 3340 / CEM 3345

Electrical Characteristics

V_{CC} = +15V V_{EE} = Internal Zener T_A = 20°C				
Parameter	Min.	Typ.	Max.	Units
Frequency Control Range	50K:1	500K:1	–	
Exponential Scale Error, Untrimmed[1]	–	0.2	1	%
Exponential Scale Error, Trimmed[1]	–	0.05	0.3	%
Multiplier Gain Error[2]	–	0.0005	0.008	%/μA
Tempo Cancellation[3]	-150	0	+150	ppm
Oscillator Drift[4]	–	±50	±200	ppm
Triangle Buffer Input Current	–	0.3	3	nA
Triangle Waveform Upper Level	4.85	5.0	5.15	V
Triangle Waveform Lower Level	-15	0	+15	mV
Triangle Waveform Symmetry	45	50	55	%
Sawtooth Waveform Upper Level	9.4	10.0	10.6	V
Sawtooth Waveform Lower Level	-25	0	+25	mV
Triangle Output Sink Capability	400	550	750	μA
Sawtooth Output Sink Capability	640	800	1000	μA
Triangle & Sawtooth Output Impedance[5]	65	100	150	Ω
Pulse Output Source Capability at +10V	2.8	3.5	4.6	mA
Squarewave Output Levels[6], CEM 3345	-1.8,-0.4	-1.3,0	-0.8,+0.4	V
PWM Input Pin Current[7]	.5	1.5	3.5	μA
PWM Input Voltage for 0% Pulse Width	-15	0	+15	mV
PWM Input Voltage for 100% Pulse Width	4.6	5.0	5.4	V
Input Bias Current at Reference and Control Current Inputs	80	200	400	nA
Tempco of Input Bias Currents	-1000	0	+1000	ppm
Offset Voltage at Reference and Control Current Inputs	-5	0	+5	mV
Hard Sync Reference Voltage	-2.3	-2.5	-2.8	V
Hard Sync Input Resistance	5	6.3	7.9	KΩ
Max Capacitor Charge/Discharge Current	400	570	800	μA
Positive Supply Current	4	5	6.5	mA
Positive Supply Voltage Range	+10		+18	V
Negative Supply Voltage Range[8]	-4.5		-18	V

Note 1: This error represents the percentage difference in scale factors (volts per frequency ratio) of the exponential generator anywhere over the exponential generator current range of 50nA to 100μA. Most of this error occurs at the range extremities.

Note 2: This error represents the percentage difference in multiplier gains at any two input currents, within the range of 20 μA to 180 μA, per μA difference between the two corresponding outputs.

Note 3: This spec represents the difference between the actual tempco of the multiplier output voltage (expressed relative to the maximum output excursions) and the tempco required to precisely cancel the tempco of the exponential scale factor (q/KT).

Note 4: The multiplier output is grounded.

Note 5: For exponential generator currents less than 10 μA; above 10 μA, impedance drops to 1/3 this value as the highest current is approached.

Note 6: With respect to the hard sync input reference voltage.

Note 7: For PWM control inputs between -1 and +6 volts. This current is significantly greater for inputs outside of this range.

Note 8: Current limiting resistor required for negative supplies greater than -6 volts.

Application Hints

Supplies

Since the device can withstand no more than 24 volts between its supply pins, an internal 6.5 volt ± 10% Zener diode has been provided to allow the chip to operate off virtually any negative supply voltage. If the negative supply is between -4.5 and -6.0 volts, it may be connected directly to the negative supply pin (pin 3). For voltages greater than -7.5 volts, a series current limiting resistor must be added between pin 3 and the negative supply. Its value is calculated as follows:

$$R_{EE} = (V_{EE} - 7.2) / .008$$

Although the circuit was designed for a positive supply of +15 volts, it may be operated anywhere between +10 and +18 volts. The only effect is on the positive peak amplitude of the output waveforms in accordance to the following: The triangle peak is one third of the supply, the sawtooth peak is two thirds of the supply, and the pulse peak is 1.5 volts below the supply.

Operation of the Temperature Compensation Circuitry

The exponential generator is temperature compensated by multiplying the current sourced into the frequency control pin (pin 15 on the CEM3340, pin 17 on the CEM3345) times a coefficient directly proportional to the absolute temperature. As this control current is applied to the exponential generator, its coefficient cancels that of the exponential generator, q/KT. This coefficient is produced by the tempco generator using the same mechanisms that create it in the exponential generator; cancellation is therefore nearly perfect.

The output of the precision multiplier (pin 14 on the 3340,

pin 16 on the 3345) internally connects to the control input of the exponential generator (base of Q_1). This output is a current and is given by:

$$I_{OM} = \frac{22V_T}{R_T}(1 - I_C R_Z/3.0)$$

where $V_T = KT/q = 26$ mV @ 20°C, and where I_C is the total current flowing into the frequency control pin and must remain positive for proper operation (a negative input current will produce the same output as a zero input current). Since the frequency control input pin is a virtual ground summing node, any number of control voltages may be summed simply with input resistors to this pin.

The current output of the multiplier is converted to the required drive voltage with a resistor from the multiplier output pin to ground. For greatest multiplier accuracy, this resistor, R_S, should be 1.8k and the current flowing out of pin 2, $22V_T/R_T$, should be close to the current flowing out of pin 1, $3.0/R_Z$.

Since the components associated with the tempco generator and multiplier determine the maximum voltage excursion possible at the base of Q_1, they should be selected to provide the desired frequency control range of the oscillator. The exponential generator itself is capable of delivering a current for charging and discharging the timing capacitor from greater than .5mA down to less than the input bias current of the buffer, thus allowing for a typical frequency range greater than 500,000:1. The most accurate portion of this current range, from 50nA to 100μA, should be used for the most critical portion of the desired frequency range.

Consideration of this critical range determines the value of C_F, the timing capacitor. The oscillation frequency is given by:

$$f = 3 I_{EG}/(V_{CC} C_F)$$

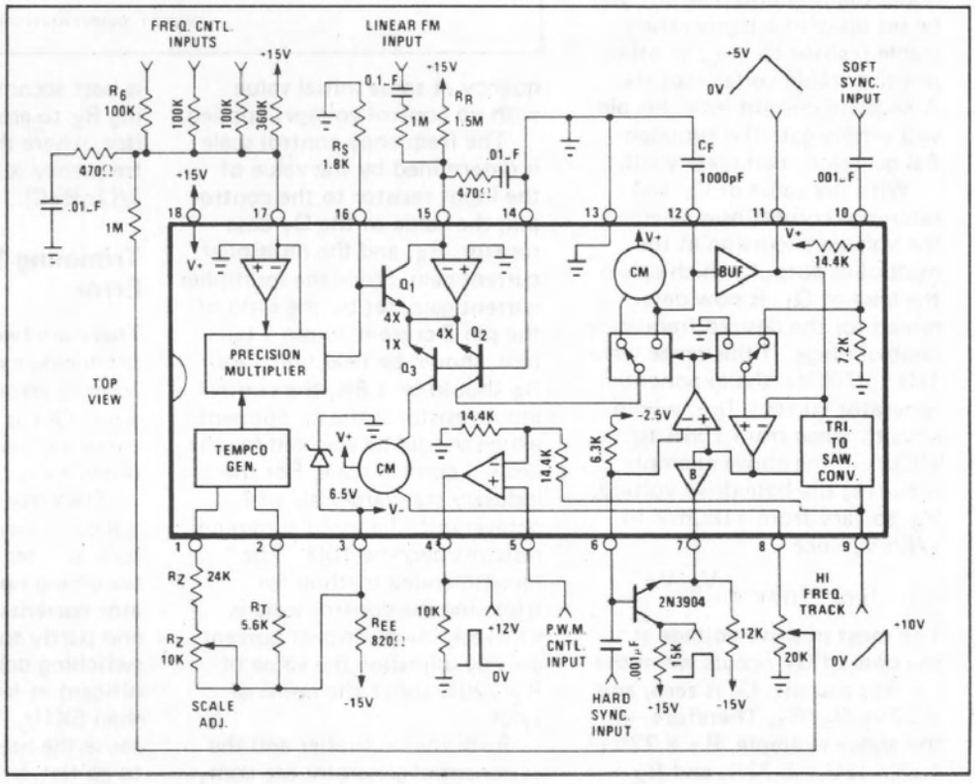
where I_{EG} is the output current from the exponential generator. If, for instance, the most important frequency range is from 5Hz to 10kHz, then C_F should be 1000pF at V_{CC} = +15V (a low leakage, low tempco capacitor, such as mica, should be used for C_F).

Next the reference current for the exponential generator (Current into pin 13 on the 3340, pin 15 on the 3345) is selected. This current ideally should be the geometric mean of the selected generator current range, but consideration of the temperature coefficient of

Absolute Maximum Ratings

Voltage Between V_{CC} and V_{EE} Pins	+24V,-0.5V
Voltage Between V_{CC} and Ground Pins	+18V, -0.5V
Voltage Between V_{EE} and Ground Pins	-6.0V,+0.5V
Voltage Between Frequency Control Pin or Reference Current Pin and Ground Pin	±6.0V
Voltage Between Multiplier Output Pin and Ground Pin	+6.0V, -1V
Current through Any Pin	±40mA
Storage Temperature Range	-55°C to +150°C
Operating Temperature Range	-25°C to +75°C

CEM 3345 Circuit Block and Connection Diagram



the bias current for op amp A2 usually dictates a higher value for the reference current. Although this bias current has been temperature compensated, it could have a worst cast tempco of 1000ppm and maximum value of 400nA. Under these conditions, a reference current of 10μA through Q_1, for instance, would have a tempco of 40ppm. It is recommended that, in general, the reference current be selected in the 3μA to 15μA range.

Since the reference current pin is a virtual ground summing node, the reference current may be set up with a temperature stable resistor to V_{CC}, or other positive stable voltage source. A negative current into this pin will simply gate the exponential generator completely off.

With the value of C_F and reference current now selected, the voltage excursion at the multiplier output, which drives the base of Q_1, is now determined for the desired frequency control range. If this range were 1Hz to 20kHz, the exponential generator current, I_{EG}, would have to range from 10nA to 200μA in the above example, requiring the base drive voltage, V_B, to vary from +180mV to -78mV, since

$$I_{EG} = I_{REF}\, e^{-V_B/V_T}$$

The most positive voltage at the base of Q_1 occurs when the control current, I_C, is zero, and is $22V_T\ R_S/R_T$. Therefore, in the above example, $R_T = 22V_T$ 1.8K/.18V = 5.72K, and R_Z = $3.0R_T/22V_T$ = 30K nominal. Finally, since the multiplier output current must range from +100μA to -43μA to produce this desired voltage excursion at the multiplier output and on the base of Q_1, the control input current, I_C, ranges from 0 to 143μA. A resistor from V_{CC} to the control input pin may be used to set the oscillator frequency at some initial value with no control voltages applied.

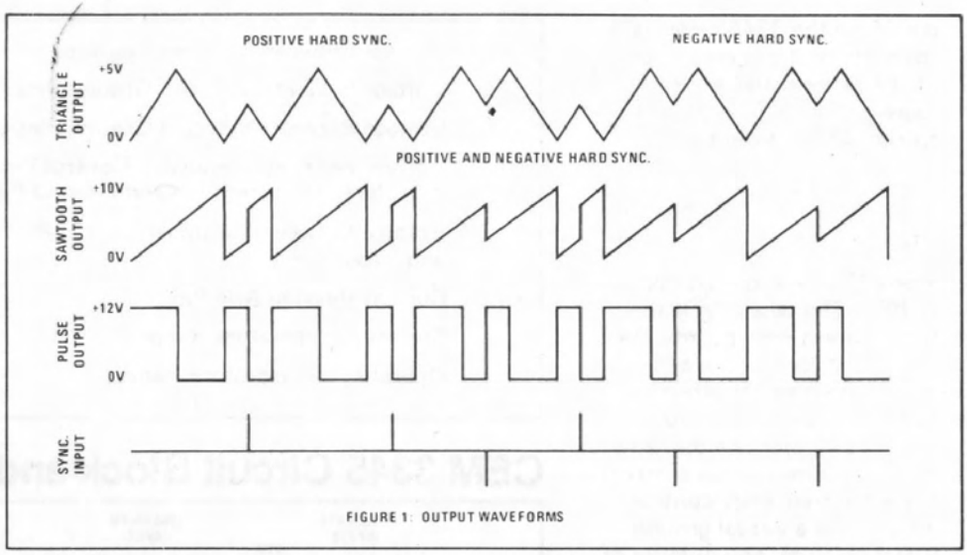


FIGURE 1: OUTPUT WAVEFORMS

The frequency control scale is determined by the value of the input resistor to the control pin, the value of the Q_1 base resistor, R_S, and the multiplier current gain. Since the multiplier current gain, set by the ratio of the pin 2 current to pin 1 current, should be near unity and R_S should be 1.8K, the control input resistor is the component which should be selected for the desired control scale. For the industry standard scale of 1 octave/volt, the input summing resistors become 100k. The recommended method for trimming the control scale is to tweek the multiplier current gain by adjusting the value of R_Z ±20% about the nominal value.

Both the multiplier and the exponential generator are compensated with the 470Ω - .01μF networks shown in the Block Diagrams and are therefore necessary in any application. Since the bandwidth of the multiplier extends beyond the audio range, it may be desirable to limit the bandwidth to reduce possible noise at the base of Q_1, thereby reducing FM noise and frequency jitter. This is best accomplished by bypassing R_S to ground with a capacitor, where the corner rolloff frequency is given by: $f_{LP} = 1/(2\pi R_S C)$.

Trimming The Scale Error

There are two basic sources producing exponential conformity error in the control scale: One is the exponential current generator and the other is the precision multiplier.

The error from the exponential converter is due partly to the bulk emitter resistance of Q_2, becoming significant at generator currents greater than 100μA, and partly to the comparator switching delay, becoming significant at frequencies greater than 5KHz. These two effects cause the oscillator frequency to go flat, but only at the uppermost octaves.

Circuitry has been provided to correct for these effects. The output of the hi-frequency track pin (pin 7 on the 3340, pin 8 on the 3345) is a current which is one fourth the generator output current, I_{EG}. This current may be converted with a grounded resistor to a voltage, a portion of which is

then fed back to the control input pin. As the frequency is increased, this feedback voltage will tend to sharpen the control scale, but only at the upper end, since the feedback voltage becomes significant only at the higher generator currents. The amount of voltage fed back is adjusted so the scale is sharpened just enough to compensate for the inherent high end flatness

The method recommended for trimming the control scale is as follows: The hi-frequency track adjust is first set so that no correction voltage is fed to the control input. The oscillator frequency is set around 200Hz and the scale adjust trimmer is adjusted for the desired scale factor (e.g. 1.000 octave/volt). Then the oscillator frequency is set to around 10KHz, and the hi-frequency track trimmer is adjusted for the same scale factor.

The source of error from the precision multiplier is due to the multiplier's gain (nominally unity) changing as the control input current changes. This type of error causes the frequency to become increasingly sharp or flat as the control current is increased. The percentage difference in multiplier gains, and hence scale factors, at any two inputs to the multiplier may be calculated as the percentage error given in the specifications times the difference in μA between the two corresponding outputs. For example, suppose the scale were adjusted for precisely 1 octave/volt at mid-range. At one octave above this adjusted octave, with the multiplier output 10μA different, the scale factor could be .08% different worst case. This would produce a volts/octave error at the base of Q_1 of .08% x 18mV = 14.4μV, which would cause this octave to be .06% (1 cent) sharp or flat. At five octaves above the adjusted octave, the scale factor could be 0.4% different worst case, producing a volts/octave error of 0.4% x 18mV = 72μV. This fifth octave would thus be 0.28% (5 cents) sharp or flat. Note that if octaves above the adjusted octaves were sharp, those octaves below the adjusted octave would become increasingly flat, and vice versa.

Typically the error produced by the multiplier is much less than the above example. However, if maintaining a tighter tolerance is required for the particular application, the multiplier error may be trimmed out for each device. The trimming procedure requires that both R_Z and R_S be made adjustable ±30% about the nominal value; R_Z is first adjusted so that the multiplier gain is constant over the selected input current range; then R_S is adjusted for the desired scale factor (adjusting R_S will reintroduce some error, so R_Z may have to be readjusted).

Should for some reason it be desired not to use the temperature compensation circuitry, the multiplier/tempco generator may be bypassed simply by leaving pin 1, pin 2, and the control input pin open, and applying the control voltage to the base of Q_1 via the multiplier output pin.

Waveform Outputs

All waveform outputs are short-circuit protected and may be shorted continuously to any supply without damaging the device. Each output, however, has differing drive capabilities.

Although the triangle output can sink at least .4mA and source over several mA, care must be exercised in loading this output. Because the output has a finite impedance and drives the comparator, a change in load will change the frequency of the oscillator. Adding a 100K resistor to ground, for instance,

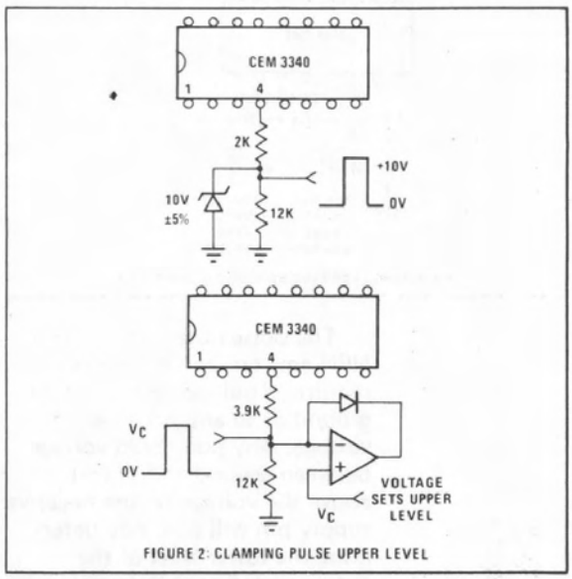


FIGURE 2: CLAMPING PULSE UPPER LEVEL

could lower the frequency by 150/100K = 0.15% (2.5 cents) worst case. A load capacitance will act like a resistor with a value $1/(2fC_L)$ and requires the same considerations as above. A continuous load no greater than 10K and/or 1000pF to ground is recommended.

Since the sawtooth output is buffer isolated from the oscillator circuitry, it can sink at least .6mA and source over several mA with no effect on oscillator performance, and only negligible effect on sawtooth waveshape. Stray capacitance at this output greater than 40pF, however, will cause a small high frequency oscillation. A 100Ω resistor between the output and load is all that is required to isolate more than .01μF.

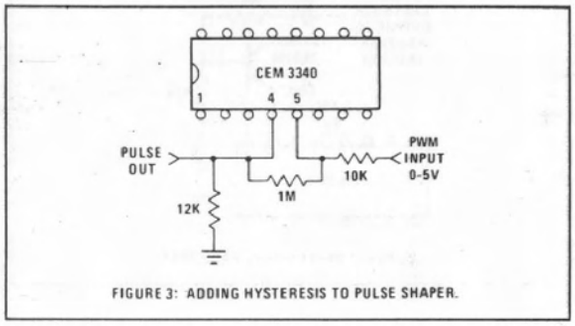


FIGURE 3: ADDING HYSTERESIS TO PULSE SHAPER.

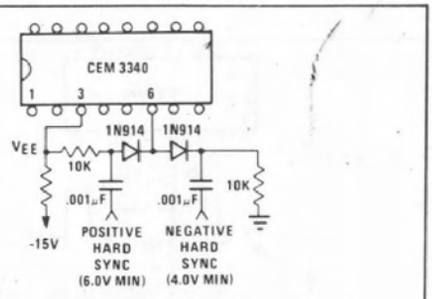


FIGURE 4: METHOD FOR SYNC ON RISING OR FALLING EDGE.

The pulse output is an open NPN emitter, and therefore requires a pull-down resistor to ground or to any negative voltage. Any pull-down voltage between ground and .5 volt above the voltage on the negative supply pin will precisely determine the lower level of the pulse wave. For pull-down voltages more negative than this, the lower level will be nearly the negative supply pin voltage. The nominal upper level of the pulse wave is given by: V_{CC} - 0.3V -1.3K • I_{PLD} for $I_{PLD} >$ 0.6mA, and V_{CC} - 0.9V for $I_{PLD} <$ 0.6mA, where I_{PLD} is the pull down current. A maximum value of 3mA for I_{PLD} is recommended. For those applications which require a more stable, well defined upper level, the circuits shown in Figure 2 may be used.

The pulse width of the pulse output may be set from 0 to 100% with a 0 to +5V external voltage (V_{CC} = +15V) applied to the PWM control input pin (pin 5 on the 3340 and 3345). The fall time of the pulse wave is slower than the rise time due to finite comparator gain. It may be speeded up considerably by adding hysteresis as shown in Figure 3. Care should be exercised in the layout to prevent stray capacitive coupling between the pulse output and the PWM input,as this can cause comparator oscillation.

The square wave output (pin 7) from the CEM 3345 also requires a pull down resistor to any negative supply greater than -4 volts. It provides an output swing from nominally 1.3 volts below the hard sync reference voltage to a level nominally the same as the hard sync reference voltage. The Block Diagram shows a convenient way of generating a full swing square wave from this output. The current pulled down from this output should also be limited to a maximum of 3mA.

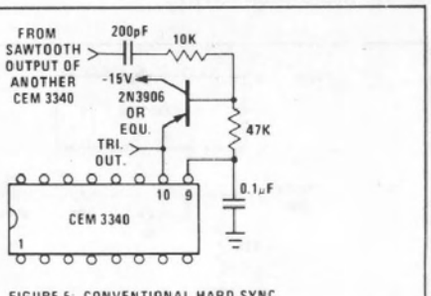


FIGURE 5: CONVENTIONAL HARD SYNC

Frequency Synchronization

The oscillator frequency may be hard synchronized in several different ways. One way is to couple positive pulses, negative pulses, or both, into the hard sync input pin (pin 6 on the 3340 and 3345). A positive sync pulse will cause the triangle wave to reverse directions only during the rising portion of the triangle, while a negative sync pulse will cause direction reversal only during the falling portion. The resulting waveforms are shown in Figure 1, and provide a wider variety of synchronized sounds than possible through conventionally synchronized oscillators. Simple capacitive coupling as shown in the Block Diagrams allows hard synchronization on both the rising and falling edge of a rectangle wave. Figure 4 shows circuitry for allowing only one or the other of the edges to synchronize the oscillator. The peak amplitude of the pulses actually appearing on the sync pin should be restricted to 1 volt minimum and 3 volts maximum for best operation.

Another method of hard synchronizing the oscillator is shown in Figure 5. Negative pulses only are coupled into the base of the PNP transistor, with a peak amplitude of 8 to 10 volts for best results at V_{CC} = +15V. This method will produce the same waveforms generated by the conventionally synchronized sawtooth oscillators.

Finally, the oscillator may be soft synchronized by negative pulses applied to the threshold voltage pin (pin 9 on the 3340, pin 10 on the 3345). These pulses cause the triangle upper peak to reverse direction prematurely, causing the oscillation period to be an integral multiple of the pulse period. The peak amplitude of these negative pulses should be limited to 5 volts maximum and positive pulses should be avoided entirely. If this input is not used for synchronization purposes, it is recommended that it be bypassed with a 0.1μF capacitor to ground to prevent synchronization or jitter to noise pulses on the V_{CC} supply line.

Linear FM

The reference current input pin may be used for linear modulation of the frequency. The external input is summed with the reference current simply through a resistor terminating at this pin. For audio FM, it is recommended that a coupling capacitor be used to prevent frequency shift when connecting to the external source. The value of the input resistor should be selected so that the maximum peak to peak input signal produces a plus and minus current equal to the reference current.

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